Design Considerations and Performance Evaluation of Single-Stage TAIPEI Rectifier for HVDC Distribution Applications

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***Abstract* — Design considerations and performance evaluations of a three-phase, four-switch, single-stage, isolated zero-voltage-switching (ZVS) rectifier are presented. The circuit is obtained by integrating the three-phase, two-switch, ZVS, discontinuous-current-mode (DCM), boost power-factor-correction (PFC) rectifier, named for short the TAIPEI rectifier, with the ZVS full-bridge (FB) phase-shift dc/dc converter. The performance was evaluated on a three-phase 2.7-kW prototype designed for HVDC distribution applications with the line-to-line voltage range from 180 V_{RMS} to 264 V_{RMS} and with a tightly regulated variable dc output voltage from 200 V to 300 V. The prototype operates with ZVS over the entire input-voltage and load-current range and achieves less than 5% input-current THD with the efficiency in the 95% range.**

I. INTRODUCTION

The HVDC distribution that has been proposed more than a decade ago is emerging as one of the most promising approaches to improve energy efficiency of data-processing and telecommunication power systems [1]-[2]. For the time being, the distribution voltage has not been standardized so that demonstration systems with nominal bus voltages ranging from 240 V to 400 V have been reported [1]-[5]. Generally, in the telecom power systems, which use -48-V dc-bus distribution, the HVDC bus architecture brings efficiency gains by lowering the distribution-bus losses, whereas in the data center power systems it increases the power system efficiency by reducing the number of conversion stages compared to the present ac-bus distribution architecture. Moreover, expected more aggressive integration of alternative energy sources into power distribution systems is making the HVDC distribution even more appealing because intrinsic dc-sources such as photovoltaic and fuel cell can be connected to the dc-bus with minimal power processing.

Generally, off-line power supplies for HVDC system consist of a front-end power-factor-correction (PFC) rectifier followed by an isolated dc-dc converter. In three-phase applications, the six-switch boost converter and Vienna rectifier are the most commonly used front-end topologies [6]. The choice of isolated dc/dc output-stage topology is primarily dependent on the power level. At kilowatt power levels, bridge-type topologies are typically used. Zero-voltage-switching (ZVS) full-bridge (FB) converter with the phase-shift control is by far the most widely employed topology in today's server power supplies and telecom rectifiers [7]. However, in high-end applications where the highest possible efficiency and power density is required, the half- or full-bridge LLC resonant topology is used [8].

Although the two-stage off-line conversion has demonstrated excellent performance, power supply designers have always been tempted to combine the two stages into a single stage to reduce the cost and/or to increase the power density [9]-[11]. Recently, a three-phase, isolated, single-stage Taipei rectifier has been introduced [12]. The rectifier is derived by integrating the three-phase, ZVS, PFC, discontinuous-conduction mode (DCM) boost rectifier, shortened to the TAIPEI rectifier [13], with a conventional phase-shift ZVS FB converter [7]. In addition to exhibiting an excellent THD and PF performance, the rectifier offers ZVS of all switches in a wide output-current range which reduces switching losses and improves efficiency.

In this paper, design considerations and performance evaluation of the three-phase single-stage Taipei rectifier for a 270-V HVDC system are presented. The performance was evaluated on a 2.7-kW prototype designed to operate in the three-phase line-to-line voltage range from 180 V_{RMS} to 264 V_{RMS} and deliver a tightly regulated dc output voltage from 200 V to 300 V. The proposed rectifier maintains input-current THD below 5% from full load down to 20% load and efficiency between 94% and 95.5% from full load down to 40% load.

II. SPECIFICATIONS

The design optimization and performance evaluation of the single-stage Taipei rectifier was performed for a prototype with the following input and output specifications:

- Line-to-line three-phase ac input voltage range: 180 V_{RMS} – 265 V_{RMS}

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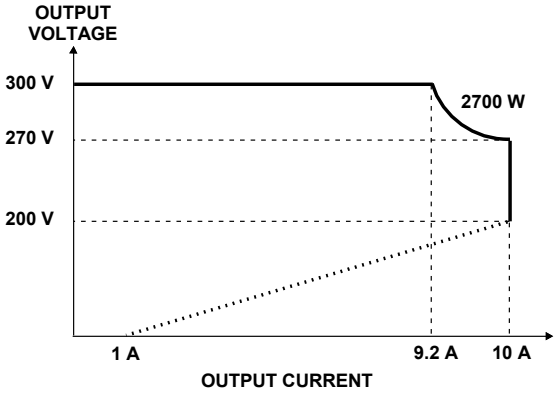

Fig. 1. Output specifications of typical HVDC power supply.

- Line frequency range: 45 Hz – 66 Hz
- THD: < 5% above 50% load, < 10% from 20% to 50% load
- PF: ≥ 99% at 100% load, ≥ 98% at 50% load
- Hold up time: ≥ 10 ms
- Efficiency: 95% from 30% to 100% load
- Output voltage: nominal 270 V, minimum 200 V, maximum 300 V (see Fig. 1)
- Output current: 10 A at 270 V (also see Fig. 1)
- Output voltage regulation: < +/- 0.25 V
- Start up or load step overshoot/undershoot: <+/- 8 V

The required output voltage, current, and power are depicted in Fig. 1. As shown in Fig. 1, the power supply delivers full power over the output voltage range from 270 V to 300 V. The output current is limited to 10 A when the output voltage is between 200 V and 270 V. When the output voltage drops below 200 V, the limit of the output current decreases linearly from 10 A to 1 A.

III. Brief Review of Single-Stage Taipei Rectifier

The circuit diagram and the ideal waveforms of the proposed three-phase, single-stage Taipei rectifier are shown in Fig. 2 and Fig. 3, respectively [12]. In this circuit, switches S_1 and S_2 simultaneously serve as the switches of the boost front end and leading-leg switches of the ZVS FB. At the input side, three boost inductors L_1, L_2, and L_3 are connected to the three-phase power-source terminals along with three differential-mode filter capacitors C_1, C_2, and C_3 connected in Y ("star") configuration. Since for a balanced three-phase power source, the potential of the common node of the filter capacitors, labeled N in Fig. 2, represents a virtual neutral. Virtual neutral N is connected to the mid-point between two switches S_1 and S_2. As a result of connecting virtual neutral N directly to the mid-point between switches S_1 and S_2, decoupling of the three input currents is achieved. In such a decoupled circuit, the current in each of the three inductors is dependent only on the corresponding phase voltage, which reduces the THD and increases the PF [13]. In addition, the

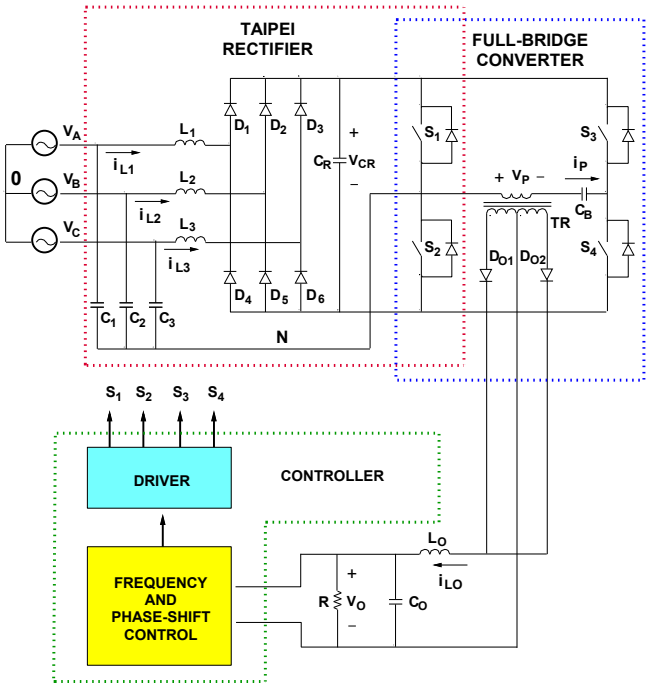

Fig. 2. Single-stage TAIPEI rectifier

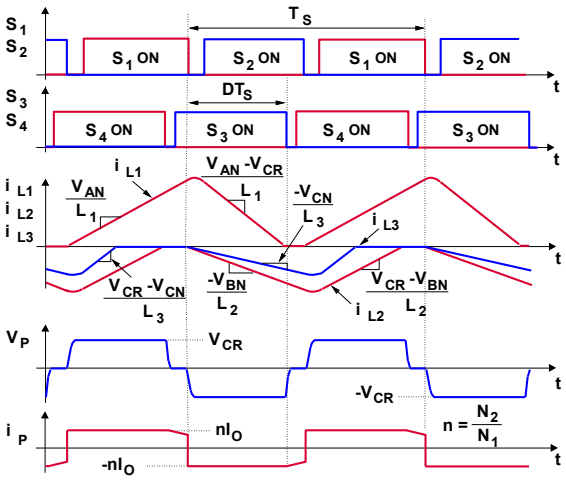

Fig. 3. Ideal waveforms of single-stage TAIPEI rectifier

mid-point of the switches does not experience abrupt changes with high dV/dt, which makes it possible for the rectifier to operate with a relatively low common-mode EMI noise.

Switches S_3 and S_4 serve as the lagging-leg switches of the phase-shift FB converter whose primary also includes isolation transformer TR and blocking capacitor C_B. In Fig. 2, the secondary-side of the FB converter is implemented with the center-tapped secondary winding, output diodes D_{O1} and D_{O2}, and output filter L_O - C_O.

Since switches S_1 and S_2 operate as the PFC boost switches as well as the leading leg switches of the ZVS FB circuit as shown in Figs. 2 and 3, the energy required to achieve ZVS of switches S_1 and S_2 is stored both in boost

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inductors L_1-L_3 and the leakage inductance of transformer TR. Because the inductance of the boost inductors is relatively large, they store enough energy for complete ZVS of switches S_1 and S_2 even at very low power levels. As a result, in the proposed circuit in Fig. 2, the leakage inductance of the transformer can be minimized. This improves the performance of the ZVS FB converter because it minimizes the secondary-side duty-cycle loss and parasitic ringing between the junction capacitance of the secondary-side rectifier and the leakage inductance [7]. The energy required to achieve ZVS of lagging-leg switches S_3 and S_4 is stored in output inductor L_O. Since the inductance of the output-filter inductor is also large, all four switches in the proposed converter can achieve ZVS in a wide input-voltage and load range.

As illustrated in Fig. 2, to achieve a tight output-voltage regulation over the entire programmable range of output voltage V_O, the proposed single-stage rectifier employs a high bandwidth frequency control assisted by the open-loop phase-shift control. The open-loop phase-shift control is employed to regulate bus voltage V_{CR} to be approximately 400 V over the entire range of output voltage V_O from 200 V to 300 V. Since for V_{CR}=400 V, duty ratio D of the full-bridge converter is

$$D = \frac{1}{n} \cdot \frac{V_O}{400}, \tag{1}$$

where $n=N_2/N_1$ is the turns ratio of transformer TR, the phase shift for a given output voltage V_O can be calculated as

$$DT_S = \frac{1}{n} \cdot \frac{V_O}{400} \cdot T_S, \tag{2}$$

where T_S is the switching period determined by the variable-frequency output-voltage control loop. Because of the required phase-shift calculations, digital control is used in this design.

It should be noted that the proposed single-stage TAIPEI rectifier is topologically identical to that described by Huang *et al.* in [11]. However, the input-current THD and efficiency performance of the two implementations are dramatically different because of different control approaches. The implementation in [11] regulates only the output voltage with a constant-frequency control that cannot achieve THD below 5% and does not provide ZVS of all four switches.

IV. Design Considerations

A. Switching Frequency Selection

Because the proposed rectifier employs variable-frequency control, the minimum and maximum switching frequencies should be selected first. The relationship between input power P_{IN}, output voltage V_O, boost inductance L, and switching frequency f_S was derived in [13] as,

$$f_S = \frac{3 \cdot V_O^2}{8 \cdot L \cdot M \cdot P_{IN} \cdot (n \cdot D)^2} \times \frac{0.48}{M - 0.92} \tag{3}$$

where input-to-output voltage conversion ratio M is

$$M = \frac{\sqrt{3} V_O}{\sqrt{2} V_{IN} \cdot n \cdot D} \tag{4}$$

and boost inductor $L = L_1 = L_2 = L_3$.

As well understood, switching frequency selection is based on the trade-off between efficiency and size, i.e., power density. In this design, the minimum frequency, which occurs at the minimum input voltage and full load is set at 18 kHz, whereas the maximum frequency is limited to 300 kHz to primarily limit the switching losses in the transformer. With the 300 kHz limit, the prototype rectifier can regulate the output voltage at high line down to 10% load. For loads below 10% of the full load, the burst-mode operation is applied.

B. Boost Inductor Design

Because the rectifier operates in DCM, the triangle-shaped currents of the boost inductors produce significantly higher core losses compared with those when the rectifier operates in the continuous-conduction mode (CCM). In addition, to maintain a low THD, it is necessary to maintain constant slopes of the boost-inductor currents. As a result, ferrite cores with an air gap are a better choice than commercially available powder cores, which exhibit higher core losses and whose permeability significantly changes under the varying magnetic field strength.

Using the relationship between input power P_{IN}, output voltage V_O, switching frequency f_S, and inductance L, shown in Eq. (3), the inductance value can be calculated as

$$L = \frac{3 \cdot V_O^2}{8 \cdot f_S \cdot M \cdot P_{IN} \cdot (n \cdot D)^2} \times \frac{0.48}{M - 0.92}. \tag{5}$$

By selecting the switching frequency of 20 kHz at the minimum input voltage and full load, which gives 2-kHz design margin, the required value of the boost inductors is approximately L=140 μH. To obtain this inductance each inductor was built using a pair of ferrite cores (PQ-40/40, DMR95) with 60 turns of Litz wire (Φ 0.1mm, 150 strands) and a 15.2 mm gap. The Litz wire was used to reduce the fringing-effect-induced winding loss near the gap of the inductor core. For this inductor design, the maximum flux density which occurs at full load and the minimum input voltage is 0.32 T.

C. Transformer Design

The transformer was built using a pair of ferrite cores (PQ-50/50, 3C96) with 42 turns of Litz wire (Φ 0.1mm, 180 strands) for primary and secondary windings. The measured magnetizing and leakage inductances are 4 mH and 6.4 μH, respectively.

Peak magnetizing current $I_{M(PK)}$ that occurs when the switching frequency is minimum is given by

$$I_{M(PK)} = \frac{V_O}{8 \cdot L_M \cdot f_{S(MIN)} \cdot n \cdot D}, \tag{6}$$

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where L_M is the magnetizing inductance of transformer TR and $f_{S(MIN)}$ is the minimum switching frequency at full load and the minimum input voltage. According to Eq. (6), the maximum peak-to-peak magnetizing current at full load and the minimum input voltage is approximately 1.88 A so that the maximum flux density in steady state is approximately 0.25 T, which gives plenty of margin with respect to the saturation flux of the ferrite core. It should be noted that blocking capacitor C_B, which is connected in series with transformer TR, eliminates any low-frequency component of the magnetizing current that may increase the flux density of the transformer.

D. Output Inductor Design

Generally, the inductance of output inductor L_O should be selected sufficiently large so that it operates in the CCM over the entire switching frequency range. In this design, output inductor L_O was built using a pair of ferrite cores (PQ-40/40, 3C96) with 72 turns of Litz wire (Φ 0.1mm, 150 strands) for each winding and a 7.2 mm gap. The measured inductance is 350 µH. The maximum flux density at steady state operation is approximately 0.27 T, which is far away from the saturation flux of the ferrite core.

E. Input Capacitor Selection

Input capacitors C_1-C_3 provide filtering of the switching-frequency ripple of the boost inductor currents and path for their low-frequency triplen harmonics. Since the magnitude of the triplen harmonic component is much smaller than that of the ac component of the boost-inductor currents, the rating of the input capacitors is essentially determined by the peak boost inductor current that occurs at the full load and low line. Since in this design, the maximum RMS current of capacitors C_1-C_3 is approximately 7.5 A, a low ESR film capacitor (2.2 µF, 630 Vdc/400 Vac, 16 A at 40 kHz and 20 A at 10 kHz) was used for each of input filter capacitors C_1, C_2, and C_3.

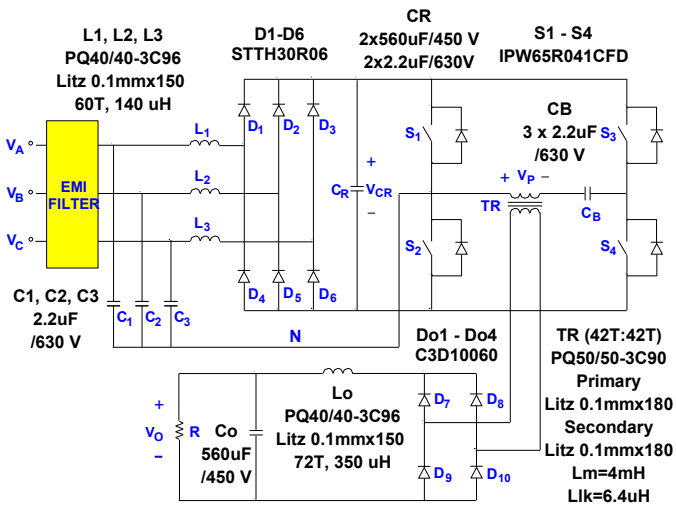

Fig. 4. Experimental prototype circuit of proposed rectifier.

F. Selection of Other Capacitors

The peak current of flying capacitor C_R is equal to the sum of the peak boost inductor current and the peak magnetizing current of transformer TR. Two parallel connected film capacitors (2.2 µF, 630 Vdc/400 Vac, 16 A at 40 kHz and 20 A at 10 kHz) were used for flying capacitor C_R. Moreover, to meet the hold-up time requirement (10 msec), two additional electrolytic capacitors (560 µF, 450 Vdc) were connected in parallel with the film capacitors.

The current through blocking capacitor C_B is equal to the magnetizing current of transformer TR and the reflected load current. Three film capacitors (2.2 µF, 630 Vdc/400 Vac, 16 A at 40 kHz and 20 A at 10 kHz) were used for blocking capacitor C_B.

Finally, two parallel connected electrolytic capacitors (470 µF, 450 Vdc) were used for output capacitors C_O.

G. Semiconductor Device Selection

Because the voltage stress of switches S_1 - S_4 is approximately equal to bus voltage V_{CR}, i.e., it is around 400 V, it is necessary to use switches that are rated at least 500-V to maintain desirable design margin of 20%. In the prototype circuit an IPW65R041CFD MOSFET (V_{DS} = 650 V, R_{DS} = 0.041 Ω, C_{OSS}=400 pF, Q_{rr}=1.9 µC) from Infineon was used for each switch. It should be noted that the body diode of the selected switch has relatively small reverse recovery charge. Because the two switches of the rectifier form totem pole configuration, the fast body diode of the switch limits shoot through current if the rectifier accidently enters CCM of operation.

Since input diodes D_1 - D_6 must block the same peak voltage stress and conduct the same peak current (approximately 28 A) as the switches, an STTH30R06 rectifier (V_{RRM} = 600 V, I_{FAVM} = 30 A) from ST was used for each diode. Since the turns ratio of transformer TR is n=1, the voltage stress of secondary-side diodes D_7 - D_{10} is equal to V_{CR}=400 V. A C3D10060 SiC rectifier (V_{RRM} = 600 V, I_{FAVM} = 10 A) from Cree was used for each output diode.

The output-voltage regulation that employs variable-frequency control together with open-loop (preprogrammed) phase-shift control was implemented by a TMS320F28027 DSP from TI.

V. Experimental Results

The performance of the proposed rectifier was evaluated on a 2.7-kW prototype circuit that was designed to operate from a 180-264 $V_{L\text{-}L(RMS)}$ three-phase input and deliver a tightly regulated programmable output voltage from 200 V to 300 V as specified in Section II.

The prototype circuit was designed with the variable-frequency-control feedback loop. Duty cycle D obtained by Eq. (1) is pre-programmed in the microcontroller to maintain

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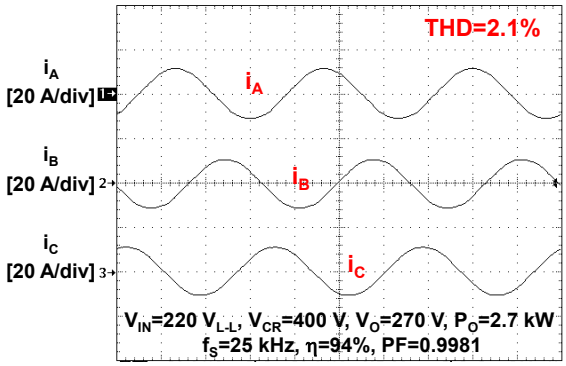

Fig. 5. Measured input current waveforms when rectifier operates from three-phase input voltage 220 $V_{L\text{-}L(RMS)}$ and delivers 2.7 kW. Time scale is 5 mS/div.

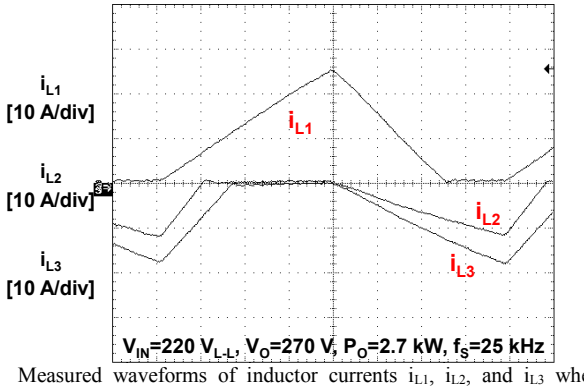

Fig. 6. Measured waveforms of inductor currents i_{L1}, i_{L2}, and i_{L3} when rectifier operates from three-phase input voltage 220 $V_{L\text{-}L(RMS)}$ and delivers 2.7 kW. Time scale is 5 μS/div.

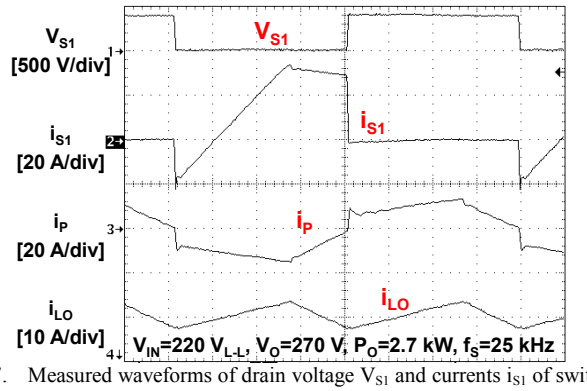

Fig. 7. Measured waveforms of drain voltage V_{S1} and currents i_{S1} of switch S_1 and primary current i_P of transformer TR when rectifier operates from three-phase input voltage 220 $V_{L\text{-}L(RMS)}$ and delivers 2.7 kW. Time scale is 5 μS/div.

flying-capacitor voltage V_{CR} at around 400 V over the output voltage range. The switching frequency range of the variable-frequency control was between 20 kHz and 300 kHz.

Figure 4 shows the power-stage schematics along with component information of the experimental prototype circuit.

Figures 5 and 6 respectively show the measured input current waveforms and current waveforms of boost inductors L_1, L_2, and L_3 of the experimental circuit at the input voltage of 220 $V_{L\text{-}L(RMS)}$ and full load. The measured input-current THD is approximately 2.1%.

Figure 7 shows drain-to-source voltage V_{S1} and drain current i_{S1} of switch S_1 together with primary current i_P and output inductor current i_{LO} when rectifier operates from three-phase input voltage 220 $V_{L\text{-}L(RMS)}$ and delivers full load. As can be seen in Fig. 7, drain current i_{S1} is negative before switch S_1 turns on. The negative current flows through the body diode of switch S_1, hence the voltage across the switch becomes zero before the switch is turned on. Switches S_2, S_3, and S_4 (not shown in Fig. 7) operate in the same manner. The experimental waveforms are in very good agreement with corresponding ideal waveforms shown in Fig. 3. The reason for a noticeable discrepancy between the measured current waveform of primary current i_P of transformer TR and corresponding ideal waveforms in Fig. 3 is the assumption that the ripple of output inductor current i_{LO} is none and voltage of the blocking capacitor is zero in the ideal case. In the prototype circuit, the peak-to-peak ac voltage across blocking capacitor C_B caused by the primary current flowing through it is around 30 V and its effect cannot be neglected. In fact, this voltage causes a relatively large decrease of the switch currents during the time intervals when the secondary winding of the transformer is shorted, because the blocking capacitor voltage resets (decreases) the transformer primary

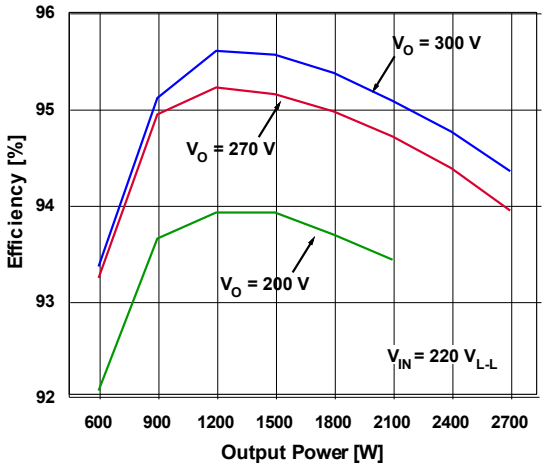

Fig. 8. Measured efficiencies of experimental PFC rectifier prototype as functions of output power.

TABLE I. Measured THD at nominal input voltage (220 $V_{L\text{-}L(RMS)}$)

THD [%]		P_O [W]							
		600	900	1200	1500	1800	2100	2400	2700
V_O [V]	200	2.49	1.03	1.94	1.61	1.67	2.00		
	270	2.89	1.22	2.40	1.32	1.82	1.73	2.14	2.06
	300	2.37	2.99	1.39	2.22	1.66	2.25	1.92	2.34

TABLE II. Measured PF at nominal input voltage (220 $V_{L\text{-}L(RMS)}$)

PF [%]		P_O [W]							
		600	900	1200	1500	1800	2100	2400	2700
V_O [V]	200	96.00	98.12	98.94	99.35	99.55	99.66		
	270	95.83	98.06	98.92	99.34	99.55	99.68	99.74	99.81
	300	92.41	95.90	97.33	98.56	99.01	99.24	99.45	99.58

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current with a relatively high rate V_{CB}/L_{LK}.

The measured efficiency, THD, and PF of the proposed rectifier as functions of output power at the line-voltage of 220 $V_{L\text{-}L(RMS)}$ are shown in Fig. 8, Table I, and Table II, respectively. The measured efficiency is between 94% and 95.5% from full load down to 40% load while the measured THD is below 5% from full load down to 20% load.

V. SUMMARY

In this paper, the three-phase, four-switch, single-stage, isolated PFC rectifier that is derived by combining the recently introduced Taipei rectifier and a conventional phase-shift full-bridge converter has been described. The proposed rectifier offers low input-current THD (< 5%) and a tightly regulated, isolated output voltage and features ZVS of all the switches over the entire input and load range. The evaluation of the proposed converter was performed on a three-phase 2.7-kW prototype operating from the 180-264-V_{RMS} line-to-line voltage range and delivering a tightly regulated programmable output voltage from 200 V to 300 V. The proposed rectifier maintains current THD below 5% from full load down to 20% load and exhibits efficiency between 94% and 95.5% from full load down to 40% load.

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