A NEW TECHNIQUE FOR REDUCING SWITCHING LOSSES IN PULSE-WIDTH-MODULATED BOOST CONVERTER

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***Abstract* — A circuit technique that reduces switching losses of the pulse-width-modulated boost converter is described. The losses are reduced by using a new switch cell that consists of an inductor, a diode, a capacitor, a main switch, and an auxiliary switch. This technique reduces the reverse-recovery-related losses of the rectifier with the inductor that controls the di/dt rate of the rectifier during its turn-off. In addition, the main switch turns off at zero current, while the auxiliary switch turns on at zero voltage. Due to the zero-current switching of the main switch, this technique is particularly suitable for boost converter implementations with insulated-gate bipolar transistors.**

I. Introduction

In single-phase applications, the boost converter is by far the most popular topology for the implementation of the front-end with power-factor correction. However, at high switching frequencies, high-voltage fast-recovery rectifiers that must be used in these applications produce significant reverse-recovery-related losses when switched under "hard" switching conditions [1]. Therefore, "hard"-switched boost power-factor-correction circuits need to be operated at relatively low switching frequencies to avoid a significant deterioration of their conversion efficiencies. Employing a soft-switching technique, the switching frequency and, therefore, the power-density of the boost front-end converter can be increased.

A number of soft-switched boost converters and their variations have been proposed in [2]-[7]. All of them use additional components to form an active snubber circuit that controls the turn-off di/dt rate of the boost rectifier.

The main feature of the active approaches introduced in [2]-[6] is that besides soft switching of the boost rectifier they also offer the zero-voltage switching (ZVS) of the boost switch. In addition, the approaches described in [4]-[6] offer soft switching of the auxiliary switch together with the boost switch. Due to ZVS of the boost switch, the efficiency of the circuits in [2]-[6] was shown to significantly improve when the boost switch is implemented with a MOSFET (metal-oxide-semiconductor field-effect transistor) device. However, the improvement in the efficiency of these circuits when used with an IGBT (insulate-gate bipolar transistor) device are expected to be significantly less because for IGBT devices zero-current switching (ZCS) is the optimal switching strategy.

The ZCS boost converter suitable for applications with IGBTs was introduced in [7]. Although in this circuit the boost switch is turned off at zero current, the circuit exhibits an undesirable resonance between the snubber inductor and the output capacitance of the switches, which requires additional clamp and/or snubber circuits [8]. The required clamp and snubber circuits not only increase the complexity and cost of the circuit, but also have a detrimental effect on its efficiency.

In this paper, a soft-switching technique which is suitable for IGBT applications and which does not suffer from undesirable resonances of circuit's components is proposed. The proposed technique improves the performance of the pulse-width-modulated (PWM) boost converter by eliminating the switching losses with a new zero-current-zero-voltage-switched (ZC-ZVS) switch cell that consists of a snubber inductor, a clamp diode, a clamp capacitor, a main switch, and an auxiliary switch. The ZC-ZVS cell reduces the reverse-recovery-related losses of the rectifier and also provides soft switching of the main and auxiliary switches. Specifically, the main switch in the proposed ZC-ZVS cell turns off with ZCS, whereas the auxiliary switch turns on with ZVS. In addition, because the proper operation of the ZC-ZVS switch cell requires that the conduction period of the main switch and the auxiliary switch overlap, the proposed switch cell is not susceptible to failures due to accidental transient overlapping of the main and auxiliary switch gate drives. Finally, the complexity and cost of the converters using the proposed technique is further reduced because the proposed ZC-ZVS switch cell requires a simple non-isolated (direct) gate drive for both switches.

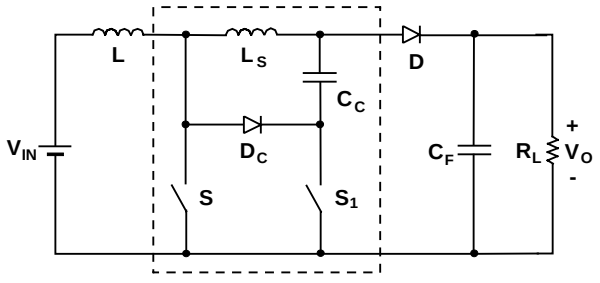

Fig. 1. Boost power stage with new ZC-ZVS cell.

II. Analysis of Operation

The circuit diagram of the boost converter that employs the new ZC-ZVS switch cell that reduces switching losses is shown in Fig. 1. The circuit in Fig. 1 uses snubber inductor L_S, which is connected in series with main switch S and rectifier D, to control the di/dt rate of the rectifier. Along with S, and L_S, auxiliary switch S_1, clamp capacitor C_C, and clamp diode D_C form a ZC-ZVS cell as indicated by dashed line in Fig. 1.

To simplify the analysis of operation, it is assumed that the inductance of boost inductor L is large so that it can be represented by constant-current source I_{IN}, and that the output-ripple voltage is negligible so that the voltage across the output filter capacitor can be represented by constant-voltage source V_O. Also, it is assumed that in the on state, semiconductors exhibit zero resistance, *i.e.*, they are short circuits. However, the output capacitance of the switches and the reverse-recovery charge of the rectifier are not neglected in this analysis. The circuit diagram of the simplified converter is shown in Fig. 2.

To further facilitate the explanation of the operation, Fig. 3 shows topological stages of the circuit in Fig. 1 during a switching cycle, whereas Fig. 4 shows the power-stage key waveforms. As can be seen from the gate-drive timing diagrams for the boost and auxiliary switches in Fig. 4, the proposed circuit operates with an overlapping gate drive of the switches where the main switch turns on and off slightly prior to the auxiliary switch, *i.e.*, both switches conduct simultaneously during the major period of the on-time and share the current.

Before main switch S is turned on at $t=T_0$, the entire input current I_{IN} flows through snubber inductor L_S and boost rectifier D. At the same time, main switch S is off blocking output voltage V_O, whereas, auxiliary switch S_1 is off blocking a voltage which is the sum of output voltage V_O and clamp-capacitor voltage V_C, *i.e.*, V_O+V_C.

After switch S is turned on at $t=T_0$, a constant voltage V_O is applied across L_S, as shown in the equivalent circuit in Fig. 3(a). As a result, inductor current i_{LS} and rectifier current i_D decreases linearly, whereas switch current i_S increases at the same rate. The rate of the rectifier current decrease is governed by

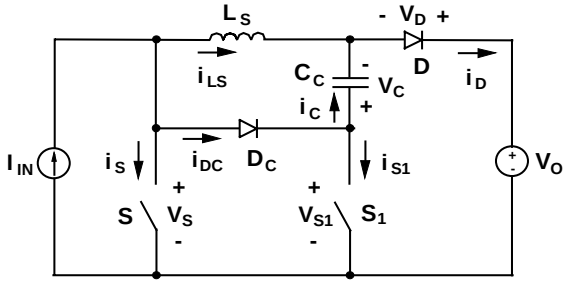

Fig. 2. Simplified circuit diagram of the proposed boost power stage showing reference directions of currents and voltages.

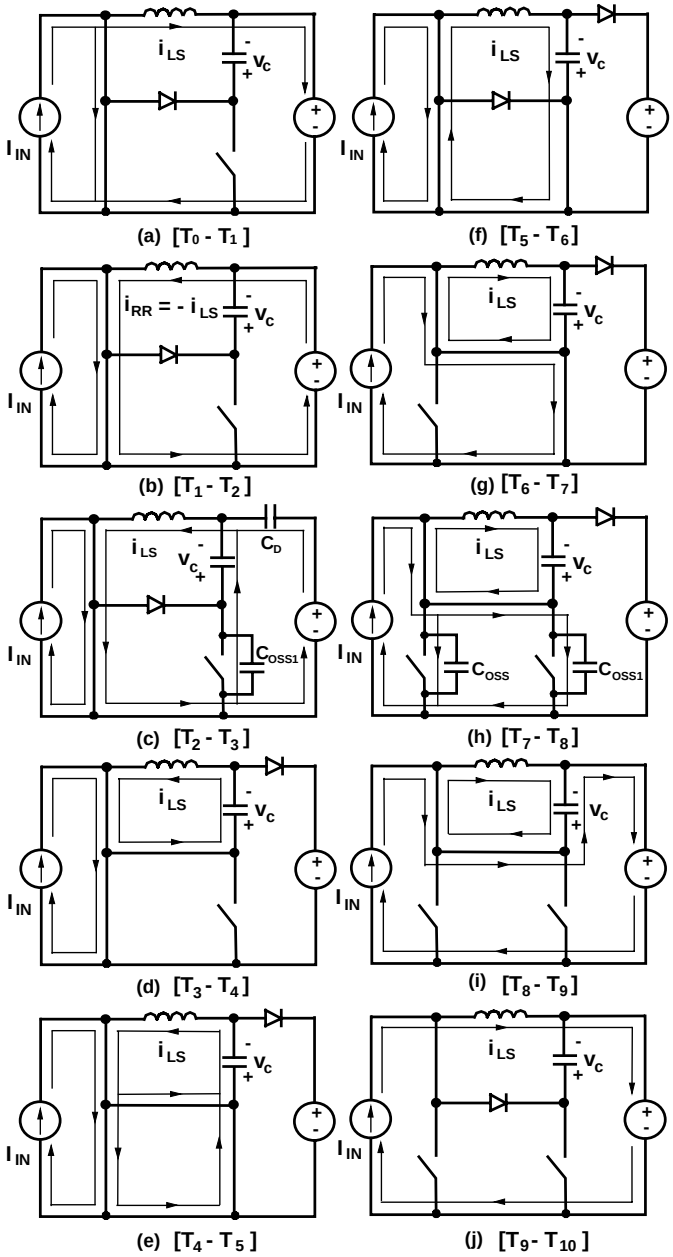

Fig. 3. Topological stages of the proposed boost power stage when the peak resonant current $I_{LS(PK)}$ is smaller than input current I_{IN}.

$$\frac{di_D}{dt} = -\frac{V_O}{L_S}. \qquad (1)$$

Since the rate of the boost-rectifier-current decrease is controlled by snubber inductance L_S, the rectifier recovered charge and the associated losses can be reduced by a proper selection of the L_S inductance. Generally, a larger inductance that gives a lower di_D/dt rate results in a more efficient reduction of the reverse recovery-associated losses [1].

At $t=T_1$, when i_{LS} and i_D decrease to zero, the entire input current I_{IN} flows through switch S, as shown in Fig. 4. Ideally,

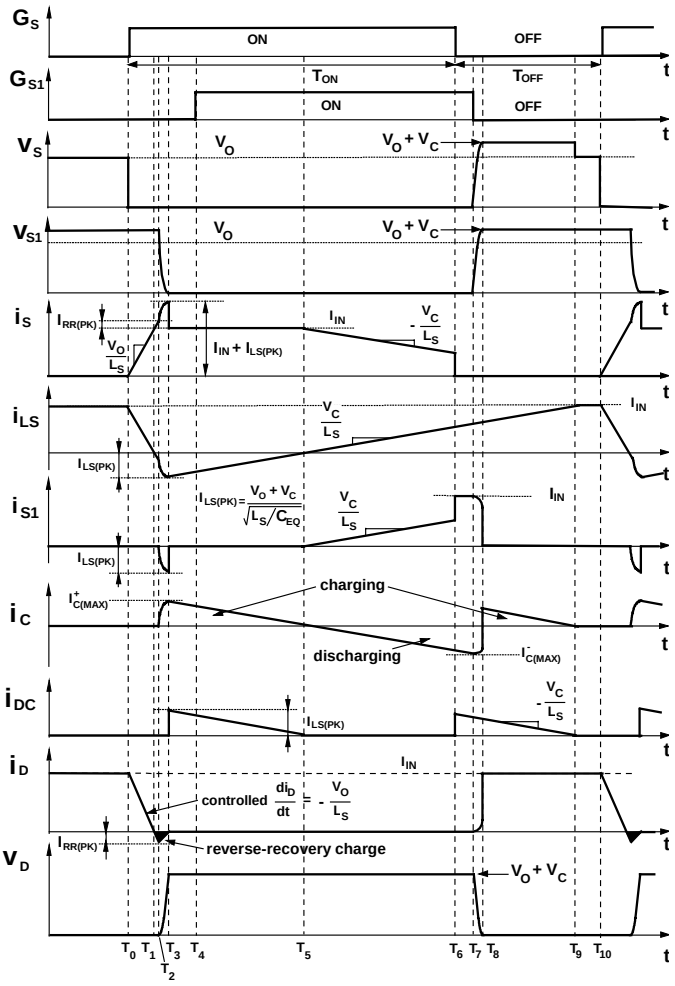

Fig. 4. Key waveforms of the proposed boost power stage when the peak resonant current $I_{LS(PK)}$ is smaller than input current I_{IN}.

when i_D falls to zero at $t=T_1$, rectifier D should stop conducting. However, due to a residual stored charge, reverse-recovery current i_{RR} will flow through rectifier D, as shown in Fig. 3(b). When, at $t=T_2$, the stored charge is recovered from the junction of rectifier D and the rectifier regains its blocking capability, a resonant circuit consisting of snubber inductor L_S, snubber capacitor C_C, output capacitor C_{OSS1} of auxiliary switch S_1, and junction capacitor C_D of rectifier D is formed, as shown in Fig. 3(c). As a result, during the T_2-T_3 interval, the drain voltage of auxiliary switch S_1 decreases from V_O+V_C to zero in a resonant fashion. At $t=T_3$, when V_{S1} falls to zero, peak resonant current $I_{LS(PK)}$, which flows in the negative direction through L_S is given by

$$I_{LS(PK)} = i_{LS}(t=T_3) = \frac{V_O + V_C}{\sqrt{L_S/C_{EQ}}}, \qquad (2)$$

where $C_{EQ} = C_{OSS1}C_C/(C_{OSS1}+C_C)+C_D \approx C_{OSS1} + C_D$ because for a properly designed circuit $C_C >> C_{OSS1}$. From Fig. 3(c), the peak current of clamp capacitor C_C at $t=T_3$, $I^+_{C(MAX)}$, is

$$I^+_{C(MAX)} = i_C(t=T_3) = \frac{C_{OSS1}}{C_{OSS1}+C_D}\frac{V_O + V_C}{\sqrt{L_S/C_{EQ}}}. \qquad (3)$$

After the voltage across auxiliary switch S_1 falls to zero at $t=T_3$, clamp diode D_C starts conducting, as shown in Fig. 3(d). When D_C is conducting, clamp capacitor voltage V_C is applied across L_S and snubber-inductor current i_{LS} increases linearly, as illustrated in Fig. 4. If the capacitance of clamp capacitor C_C is large, capacitor voltage V_C is almost constant so that inductor current i_{LS} increases and capacitor current i_C decreases linearly, *i.e.*, $di_{LS}/dt = -di_C/dt = V_C/L_S$. Otherwise, i_{LS} and i_C change in a resonant fashion. This topological stage ends at $t=T_5$, when i_C reaches zero and clamp diode D_C stops conducting. As can be seen from Fig. 4, to achieve ZVS of auxiliary switch S_1, it is necessary to turn on S_1 before $t=T_5$, *i.e.*, S_1 should be turned on while clamp diode D_C is conducting. In Fig. 4, auxiliary switch S_1 is turned on at $t=T_4$. It should be noted that after $t=T_4$, current i_{LS} or a part of it may continue flowing through S_1 depending on the relative values of on-impedances of S_1 and D_C, as shown in Fig. 3(e). Since auxiliary switch S_1 starts conducting after clamp diode D_C ceases to conduct at $t=T_5$, auxiliary-switch current i_{S1} continues to increase linearly, as illustrated in Fig. 3(f). At the same time, main-switch current i_S decreases at the same rate because the sum of i_{S1} and i_S is equal to the constant input current I_{IN}.

When main switch S is turned off at $t=T_6$, the current which was flowing through switch S is diverted to auxiliary switch S_1 through clamp diode D_C as shown in Fig. 3(g). It should be noted that at the moment of switch S turn-off at $t=T_6$, the current of S is smaller than I_{IN}, as shown in Fig. 4. In addition, the voltage across switch S during its turn-off is clamped to zero by conducting clamp diode D_C and auxiliary switch S_1, as can be seen from Fig. 3(g). As a result, switch S is turned off with much reduced current and with zero voltage. In fact, the circuit can be designed to achieve complete ZCS of main switch S during the turn-off time, as it will be discussed later. During the T_6-T_7 interval, input current I_{IN} flows through S_1, whereas C_C continues to discharge through L_S. This interval ends at $t=T_7$ when auxiliary switch S_1 is turned off. It should be noted that auxiliary switch S_1 shares the input current with main switch S during the time interval between $t=T_5$ and $t=T_6$, as shown in Fig. 3(f) and Fig. 4. Therefore, by the addition of auxiliary switch S_1, the overall rms current of main switch S is reduced.

After switch S_1 is turned off at $t=T_7$, current I_{IN} flowing through switch S_1 is diverted from the switch to its output capacitance C_{OSS1}, as shown in Fig. 3(h). As a result, the voltage across auxiliary switch S_1 starts to increase linearly from zero to V_O+V_C due to the constant charging current I_{IN}. At the same time, because of conducting D_C, voltage V_S of main switch S also increases from zero towards $V_O + V_C$. When the voltage across switches S and S_1 reaches $V_O + V_C$ at $t=T_8$, rectifier D starts conducting, as shown in Fig. 3(i). During the T_8-T_9 time interval, i_{LS} continues to increase

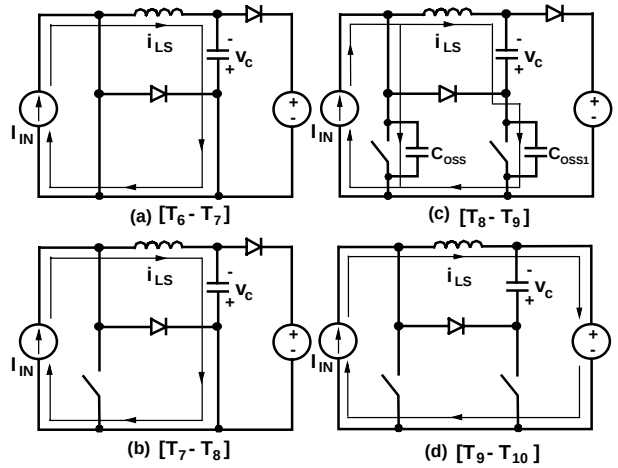

Fig. 5. Topological stages of the proposed boost power stage when I_{IN} is smaller than the peak resonant current $I_{LS(PK)}$.

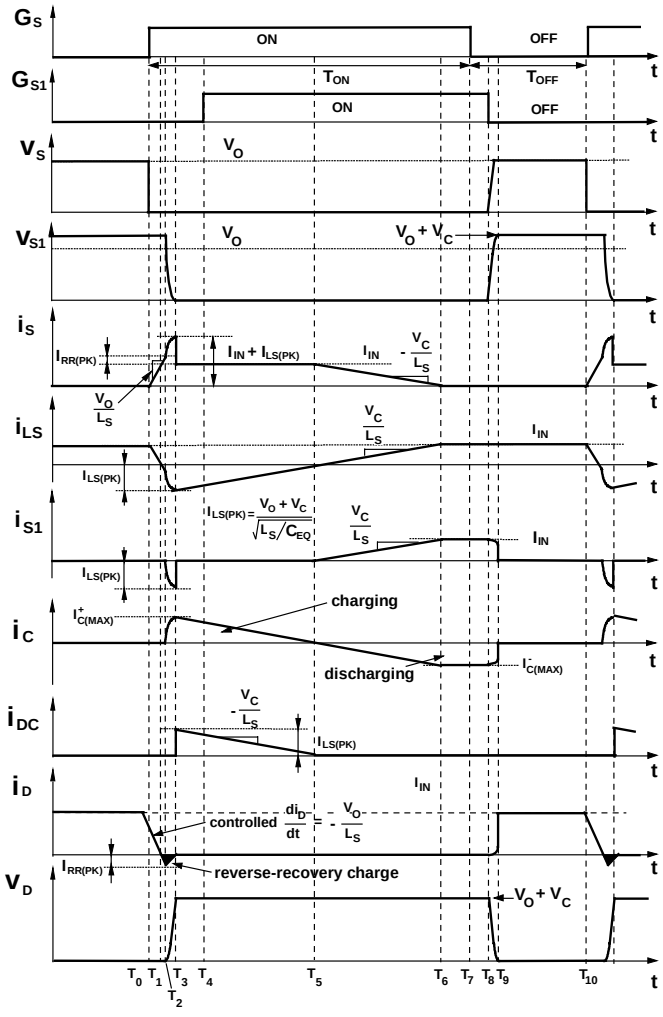

Fig. 6. Key waveforms of the proposed boost power stage when I_{IN} is smaller than the peak resonant current $I_{LS(PK)}$.

toward I_{IN}, while clamp capacitor C_C is being charged by the difference of input current I_{IN} and snubber inductor current i_{LS}, *i.e.*, by $I_{IN} - i_{LS}$. When, at $t=T_9$, i_{LS} reaches I_{IN}, clamp diode D_C stops conducting and the entire input current flows through D, as shown in Fig. 3(j). The circuit stays in this topological stage until the next switching cycle is initiated at $t=T_{10}$.

At light load operation, when input current I_{IN} is smaller than the peak resonant current $I_{LS(PK)}$ described in Eq. (2), the charge balance of clamp capacitor C_C is completed during switch-on period. Figures 5 and 6 show the power-stage operation when I_{IN} is smaller than $I_{LS(PK)}$. Figure 5 shows topological stages during a switching cycle, whereas Fig. 6 shows the power-stage key waveforms.

During the T_0-T_5 interval, the key waveforms and power-stage operation when I_{IN} is smaller than $I_{LS(PK)}$ are the same as in the case when I_{IN} is greater than $I_{LS(PK)}$, Figs. 3 and 4. However, after $t=T_5$, the operation when I_{IN} is smaller than $I_{LS(PK)}$ is different from that shown in Fig. 3 and 4. Since when I_{IN} is smaller than $I_{LS(PK)}$, snubber-inductor current i_{LS} reaches I_{IN} level before main switch S turned off at $t=T_6$, auxiliary switch S_1 carries the entire input current during the T_6-T_8 interval as shown in Fig. 6. Therefore, to achieve a complete ZCS of the main switch, the peak resonant current $I_{LS(PK)}$ should be designed to be greater than input current I_{IN} over the entire load and line range.

III. Design Considerations

As can be seen from the waveforms in Fig. 4, to achieve a complete ZCS turn-off of main switch S, it is necessary that current through clamp capacitor i_C at the moment when S is turned off is equal to input current I_{IN}, *i.e.*,

$$i_C(t=T_6) = I_{IN}. \tag{4}$$

Moreover, since for a properly designed circuit the T_6-T_7 time interval is much shorter than the T_5-T_6 time interval in Fig. 4, the value of clamp capacitor current i_C at $t=T_6$ and $t=T_7$ is approximately the same, *i.e.*,

$$i_C(t=T_6) \approx i_C(t=T_7) = I^{-}_{C(MAX)}. \tag{5}$$

where $I^{-}_{C(MAX)}$ is the maximum discharging current, as indicated on the i_C waveform in Fig. 4. From Eqs. (4) and (5), the ZCS condition for S can be defined as

$$I^{-}_{C(MAX)} = I_{IN}. \tag{6}$$

Since for the circuit design wherein $I^{-}_{C(MAX)} = I_{IN}$, C_C charging occurs only during the T_2-T_5 interval, *i.e.*, the charging interval T_8-T_9 shown in Fig. 4 does not exist, the charge balance of C_C requires that

$$I^{+}_{C(MAX)} = i_C(t=T_3) \approx I^{-}_{C(MAX)} \approx I_{IN}. \tag{7}$$

From Eqs. (4) and (7), the ZCS condition can be written as

$$\frac{1}{C_{OSS1}}\sqrt{L_S(C_{OSS1}+C_D)} \le \frac{V_O+V_C}{I_{IN}}. \tag{8}$$

If Eq. (8) is satisfied at the maximum power, *i.e.*, for $I_{IN}=I_{IN(MAX)}$, complete ZCS of switch S is achieved in the full load range. It should be noted that because auxiliary switch S_1 and rectifier D are both turned on under ZVS condition,

external capacitance can be added across S_1 or D without incurring additional switching losses. If it is necessary to satisfy Eq. (8) for given V_O, $I_{IN(MAX)}$, L_S, V_C, and for given C_{OSS1} and C_D, external capacitance can be added in parallel with C_{OSS1} or C_D. However, since main switch S is always turned off with ZVS, the complete ZCS of main switch S is not necessary to improve overall performance of the converter. Therefore, the main switch current during turn-off (at $t=T_6$ in Fig. 4) needs to be optimized so that the peak resonant current $I_{LS(PK)}$ is not excessive.

As can be seen from Fig. 4, the voltage stress of main switch S, auxiliary switch S_1, and rectifier D is $V_O + V_C$. Therefore, the voltage stress of main switch S in the proposed converter is higher compared to the corresponding stress in the conventional, "hard"-switched boost converter. To keep the voltage stress of switch S and switch S_1 within reasonable limits, it is necessary to properly select clamp-voltage level V_C.

The derivation of V_C dependence on the circuit parameters can be simplified by recognizing that in the boost converter in Fig. 1 that is designed to minimize the reverse-recovery-related losses and achieve complete ZCS of main switch S, the rectifier-current commutation interval T_0-T_2 is much shorter than on-time period T_{ON} of switch S, and that capacitor charging period T_8-T_9 is zero. In addition, the duration of the commutation periods T_2-T_3 and T_7-T_8 are negligible compared to the on-time interval of main switch S.

From Fig. 4, it can be seen that, from $t=T_3$ to $t=T_5$, clamp capacitor C_C is charged with current i_C which has a constant slope of $di_C/dt = V_C/L_S$. Therefore, since the circuit is designed to achieve ZCS of main switch S, $i_C(t=T_3) = I^+_{C(MAX)} = I_{IN}$, and since the duration of the time interval from $t=T_2$ to $t=T_5$ is approximately one-half of the on-time of switch S, clamp-capacitor voltage V_C can be expressed as

$$V_C \approx L_S \frac{I_{IN}}{DT_S/2} = 2\frac{L_S f_S I_{IN}}{D}, \qquad (9)$$

where D is the duty-cycle of switch S, T_S is the switching period, and f_S is the switching frequency. Since for a lossless boost power stage for which the current commutation interval T_0-T_2 is much shorter than T_{ON}, the voltage-conversion ratio V_O/V_{IN} is given by

$$\frac{V_O}{V_{IN}} = \frac{I_{IN}}{I_O} = \frac{1}{1-D}. \qquad (10)$$

Eq. (10) can be written as

$$V_C \approx 2L_S f_S I_O \left(\frac{V_O^{\,2}}{(V_O - V_{IN})V_{IN}} \right). \qquad (11)$$

According to Eq. (11), V_C is maximum at full load $I_{O(MAX)}$ and high line $V_{IN(MAX)}$. For given input and output specifications, *i.e.*, for given $I_{O(MAX)}$, $V_{IN(MAX)}$, and V_O, clamp-capacitor voltage V_C can be minimized by minimizing the $L_S f_S$ product.

It should be noted that the control of the proposed boost converter can be implemented in the same way as in its conventional "hard" switched counterpart as long as an additional gate-drive circuit is provided. Specifically, in the input-current-shaping applications, the proposed converter can be implemented with any known control technique, such as average current, peak current, or hysteretic control.

Finally, the proposed ZC-ZVS cell can be applied to any member of the PWM-converter family. As an example, Fig. 7 shows an implementation of this technique in the three-phase rectifier.

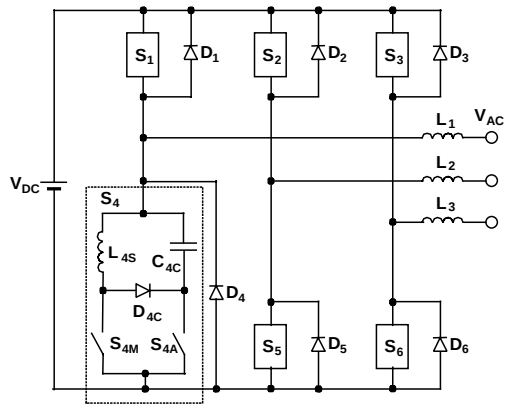

Fig. 7. Three-phase rectifier with ZC-ZVS cells.

IV. Experimental Results

The performance of the boost converter with the proposed ZC-ZVS cell was evaluated on a 1-kW (375 V/ 2.67 A), universal-line-range (90 - 265 V_{ac}) power-factor-correction circuit operating at 80 kHz. The experimental circuit was implemented with the following components: boost switch S - IXGK50N60B; auxiliary switch S_1 – HGTG20N60B; boost rectifier D = two RHRP3060 connected in parallel; boost inductor L = 0.8 mH; snubber coupled inductor L_S = 3.3 μH; snubber rectifier D_C - RHRP3060, clamp capacitor $C_C = 2 \times 6.8$ μF / 100 V connected in parallel, and bulk capacitor $C_F = 2 \times 470$ μF / 450 V connected in parallel.

Boost inductor L was built using toroidal cores (Magnetics, Kool Mu 77439-A7, two cores in parallel) and 55 turns of AWG#14, whereas snubber inductor L_S was built with a toroidal core (Kool-Mu 77312-A7) with 13 turns of AWG#14. With the selection of L_S = 3.3 μH, the di/dt rate of the rectifier during the turn-off period was limited to $di_D/dt = V_O/L_S$ = 114 A/μs. The control circuit was implemented with an average-current PFC controller UC3854. A TC427 driver is used to generate the required gate-drive signals for the main and auxiliary switches.

Figure 8 shows the measured efficiencies of the experimental converter with and without the ZC-ZVS active snubber at the minimum and the maximum line voltages as functions of the output power. As can be seen from Fig. 8, the active snubber improves the conversion efficiency over the entire load range for both line voltages. Nevertheless, the

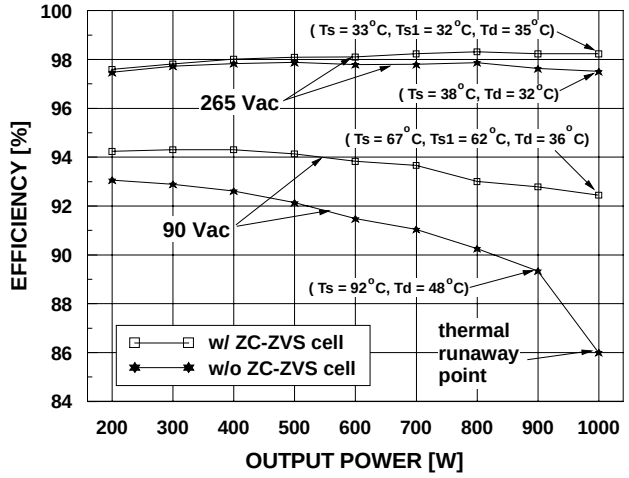

Fig. 8. Measured, full-power efficiencies of the experimental converter with and without a ZC-ZVS cell at the minimum and maximum line voltages as functions of the output power.

efficiency improvement is more pronounced at the minimum line and higher power levels where the reverse-recovery losses are greater. Specifically, at the maximum line (265 V_{ac}), the efficiency improvement at 1 kW is 0.7%. However, at the minimum line, the implementation without the active snubber cannot deliver more than approximately 900 W due to the thermal runaway of the diode caused by the excessive reverse-recovery loss. At P_O=900 W, the active snubber improves the efficiency by approximately 3%, which translates into approximately 30% reduction of the losses. In fact, for the implementation without ZC-ZVS cell the temperature of the boost switch is T_S=92°C at 900 W, which is significantly higher than the temperature of the main switch (T_S=67°C) in the implementation with the ZC-ZVS cell at 1 kW.

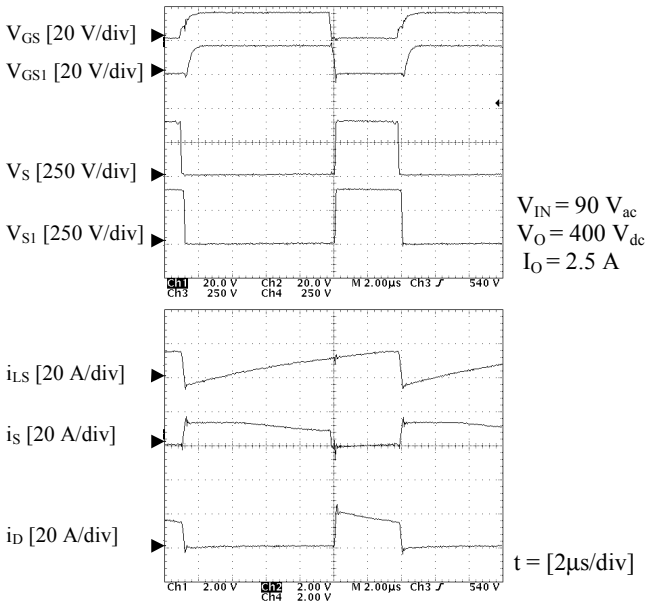

Fig. 9. Oscillograms of gate-drive voltages V_{GS} and V_{GS1}, main switch voltages V_S and V_{S1}, and snubber inductor currents i_{LS}, switch current i_S, and doide current i_D.

Finally, Fig. 9 shows the gate drives, main switch voltage, and current waveforms of the prototype at low line and full load. It can be seen that the main switch turns off with ZVS and low current condition.

V. Summary

A technique that improves the performance of the PWM boost converter by eliminating the switching losses with a new ZC-ZVS switch cell is described. The ZC-ZVS cell, which consists of an inductor, a capacitor, a diode, a main switch, and an auxiliary switch reduces the reverse-recovery-related losses of the rectifier, and also provides zero-current turn-off of the main switch and zero-voltage turn-on of the auxiliary switches. Due to the zero-current switching of the main switch, the proposed technique is suitable for IGBT implementations.

A complete explanation of operation of and design guidelines for the boost converter with the proposed ZC-ZVS cell are provided. The performance of the proposed technique was evaluated on a 1-kW, universal-input, PFC boost rectifier prototype.

References

[1] Y. Khersonsky, M. Robinson, D. Gutierrez, "New fast recovery diode technology cuts circuit losses, improves reliability," *Power Conversion & Intelligent Motion (PCIM) Magazine*, pp. 16 - 25, May 1992.

[2] R. Streit, D. Tollik, "High efficiency telecom rectifier using a novel soft-switched boost-based input current shaper," *International Telecommunication Energy Conf. (INTELEC) Proc.*, pp. 720 - 726, Oct. 1991.

[3] G. Hua, C.S. Leu, F.C. Lee, "Novel zero-voltage-transition PWM converters," *IEEE Power Electronics Specialists' Conf. (PESC) Rec.*, pp. 55 - 61, June 1992.

[4] J. Bassett, "New, zero voltage switching, high frequency boost converter topology for power factor correction," *International Telecommunication Energy Conf. (INTELEC) Proc.*, pp. 813 - 820, Oct. 1995.

[5] M.M. Jovanović, "A technique for reducing rectifier reverse-recovery-related losses in high-voltage, high-power boost converters," *IEEE Applied Power Electronics (APEC) Conf. Proc.*, pp. 1000 - 1007, Mar. 1997.

[6] C.M.C. Duarte, I. Barbi, "An improved family of ZVS-PWM active-clamping dc-to-dc converters," *IEEE Power Electronics Specialists' Conf. (PESC) Rec.*, pp. 669 - 675, May 1998.

[7] G. Hua, X. Yang, Y. Jiang, F.C. Lee, "Novel zero-current-transition PWM converters," *IEEE Power Electronics Specialists' Conf. (PESC) Rec.*, pp. 538 - 544, June 1993.

[8] K. Wang, G. Hua, F.C. Lee, "Analysis, design and experimental results of ZCS-PWM Boost Converters," *International Power Electronics Conf. Proc.*, pp. 1202-1207, Yokahama, Japan, April 1995.