Generalized Topologies of Single-Stage Input-Current-Shaping Circuits

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Abstract—In this paper, two generalized topologies of single-stage input-current-shaping (S2ICS) circuits are derived: S2ICS circuits with two-terminal ICS cells and S2ICS circuits with three-terminal ICS cells. It is shown that most of the recently published S2ICS circuits belong to either of the two generalized topologies. It is also shown that the two generalized S2ICS topologies are functionally equivalent. Based on the generalized approach, a few new S2ICS circuits are developed. Experimental results obtained on a selected pair of S2ICS circuits with two-terminal and three-terminal ICS cells are also provided.

Index Terms—Generalization, line current shaper, power factor correction, single-stage ac–dc conversion.

I. INTRODUCTION

A NUMBER of single-stage input-current-shaping (S2ICS) converters have been introduced recently [1]–[10]. Unlike the two-stage converters with input-current shaping (ICS), in a S2ICS converter, the ICS switch and its controller are saved and ICS, isolation, and high-bandwidth output-voltage control are performed in a single conversion step, i.e., without creating a regulated dc bus. All these S2ICS circuits integrate a boost ICS stage with a forward or flyback dc/dc-converter stage. The ICS inductor of a S2ICS circuit can operate either in the discontinuous conduction mode (DCM) or in the continuous conduction mode (CCM). In the CCM operation of the ICS inductor, low line-current harmonic distortions are achieved because of the inherent property of the DCM boost converter to draw a near sinusoidal current if its duty cycle is held relatively constant during a half line cycle. The implementation of the CCM operation of the ICS inductor is more challenging because a single switch has to control two different duty cycles; i.e., a constant duty cycle of the dc/dc-converter (in steady state) and a variable duty cycle of the ICS inductor. Usually, the DCM operation gives a lower total harmonic distortion (THD) of the line current compared to the CCM operation. However, the CCM operation yields a slightly higher efficiency compared to the DCM operation. A detailed review of the S2ICS converters is presented in [11].

Generally, S2ICS converters meet European and/or Japanese regulatory requirements regarding line current harmonics, but they do not improve the power factor (PF) and reduce the THD as much as their conventional two-stage counterparts. Typically, PF for the S2ICS converters is between 0.8 and 0.9, whereas their THD is in the 40–75% range.

In order to better understand the differences and similarities between different S2ICS circuits as well as to develop new S2ICS topologies, a generalization of the S2ICS circuits is performed in this paper. It is shown that most of the recently published S2ICS circuits can be classified in two families: the S2ICS family with three-terminal ICS cells and the S2ICS family with two-terminal ICS cells. It is shown that, although topologically different, the two S2ICS families are functionally equivalent and exhibit very similar performance. Advantages and disadvantages of the two S2ICS families are discussed. Using the generalized approach, a few new S2ICS circuits are developed. Finally, experimental results obtained on a selected pair of S2ICS circuits with two-terminal and three-terminal ICS cells are provided.

II. GENERALIZED S2ICS TOPOLOGIES

A. S2ICS Family with Three-Terminal ICS Cells

A typical S2ICS circuit with DCM operation of the ICS inductor is shown in Fig. 1 [4]. In this circuit, a boost ICS stage and a flyback or forward dc/dc converter stage are combined into a single stage. The ICS cell, shown in the dotted rectangle in Fig. 1, includes boost inductor $L_B$ and two current paths: path $XZ$ for charging $L_B$ when switch $S$ is on and path $XY$ for discharging $L_B$ when switch $S$ is off. Since charging path $XZ$ is connected to switch $S$ and discharging path $XY$ is connected to bulk capacitor $C_B$, the ICS cell in Fig. 1 has three terminals. The function of the transformer winding $N_1$ is to limit the voltage on bulk capacitor $C_B$ and to improve the overall efficiency. In fact, when switch $S$ is closed, the induced voltage across winding $N_1$ is in opposition to the rectified line voltage; as a result, to keep the same volt-second product across $L_B$, a larger duty cycle is necessary. With a larger duty cycle and the inductor of the dc/dc power stage operating in CCM, the bulk-capacitor voltage is reduced. However, winding $N_1$ also introduces line-current distortions around the zero crossings because the line current cannot flow when the instantaneous line voltage is lower than the voltage induced across winding $N_1$. Therefore, in the S2ICS circuit in Fig. 1 there is a strong trade-off between PF, THD, and efficiency. To further reduce the bulk capacitor voltage and improve efficiency, another transformer winding, $N_2$, can be placed in discharging path $XY$ [5] as shown in Fig. 2. During the discharging of the ICS inductor, the voltage across windings
$N_2$ has the same direction as the voltage across the bulk capacitor, i.e., winding $N_2$ effectively increases the reset voltage across the ICS inductor. As a result, the required reset voltage for $L_B$ can be obtained with a lower voltage on bulk capacitor $C_B$. It should be noted that since windings $N_1$ and $N_2$ are magnetically coupled to the secondary winding of transformer $TR$, they can be used to directly transfer energy from the input (line) to the load. Winding $N_1$ provides direct energy transfer with the forward-type dc/dc power stages, while winding $N_2$ provides direct energy transfer with the flyback-type dc/dc power stages. Generally, direct energy transfer improves the conversion efficiency.

To achieve CCM operation of the ICS inductor, an additional inductor or capacitor is required as shown in Figs. 3 [6], [8], [9] and 4 [1], respectively. The function of inductor $L_4$ in Fig. 3 and capacitor $C_1$ in Fig. 4 is to provide a variable effective duty cycle for boost inductor $L_B$ even when the duty cycle of switch $S$ is relatively constant during a half line cycle. Namely, to achieve a good tracking of the line current and line voltage with boost inductor $L_B$ operating in CCM, it is necessary that the duty cycle of $L_B$, $D_{LB}$, defined as the ratio of the charging time of $L_B$ and the switching period, is proportional to the instantaneous line voltage during a half line cycle. Specifically, $D_{LB}$ should be maximum around the zero crossings of the line voltage and minimum around the line voltage peaks, i.e.,

$$D_{LB} \approx 1 - \frac{|V_{so}|}{V_B}. \quad (1)$$

Inductor $L_4$ in Fig. 3 modulates boost-inductor duty cycle $D_{LB}$ by delaying the commutation of the boost inductor current from path $XY$ to path $XZ$ after switch $S$ is turned on. Namely, after switch $S$ is turned on, boost-inductor current charges capacitor $C_1$ until $C_1$ is charged to $V_B$. Once $C_1$ is charged to $V_B$, the boost-inductor current commutates to path $XY$. As a result, duty cycle $D_{LB}$ is different from the duty cycle of switch $S$. Furthermore, since the charging time of $C_1$ is proportional to the boost-inductor current, $D_{LB}$ varies with the line voltage as shown in (1).

In all $S^2$ICS circuits in Figs. 1–4, the three-terminal ICS cell, shown in the dotted rectangle, has the same basic topology that includes ICS inductor $L_B$ connected to the output of the full-bridge rectifier, $L_B$ charging path $XZ$ connected to switch $S$, and $L_B$ discharging path $XY$ connected to bulk capacitor $C_B$. Therefore, all $S^2$ICS circuits in Figs. 1–4 can be represented by a $S^2$ICS circuit with a generalized three-terminal ICS cell as shown in Fig. 5. The generalized three-terminal ICS cell in Fig. 5 consists of ICS inductor $L_B$, the boost inductor charging path $P_{ch}$ between nodes $X$ and $Z$, and the boost inductor discharging path $P_{dch}$ between nodes $X$ and $Y$. The $L_B$ charging and discharging paths each includes at least one of the following components: a diode, a transformer winding, an inductor, and a capacitor.

Using this generalized approach, it can be concluded that the charging and discharging paths of the boost inductor can be implemented with many different combinations of diodes, inductors, capacitors, and additional windings of the transformer in the dc/dc power stage. A number of possible new implementations of the three-terminal ICS cells are shown in Fig. 6.
should be noted that in all implementations of the three-terminal ICS cell in Fig. 6, boost inductor $L_B$ operates in the CCM: CCM operation of $L_B$ is achieved by additional capacitor $C_1$ in Fig. 6(a), and by both additional inductor and capacitor in Fig. 6(b)–(d).

Finally, it should be noted that windings $N_2$ and $N_3$ in Figs. 1–6 can be implemented by tapping the primary winding of the power transformer [8]–[10]. As an example, Fig. 7 shows the implementation of winding $N_1$ in the three-terminal ICS cell in Fig. 3 as a portion of the primary winding of transformer. While tapping simplifies the transformer design, it has no effect on the operation of the $S^2$ICS circuits.

### B. $S^2$ICS Family with Two-Terminal ICS Cells

Another implementation of the DCM $S^2$ICS circuit is shown in Fig. 8 [3]. The $S^2$ICS circuit in Fig. 8 can be redrawn as shown in Fig. 9. In this implementation, a two-terminal ICS cell, shown in the dotted rectangle, is inserted between the full-bridge rectifier and the bulk capacitor. The two-terminal ICS cell in Fig. 9 consists of ICS inductor $L_B$, the charging path of $L_B$ (the path with $D_1$ and $N_1^*$), and the discharging path of $L_B$ (the path with $D_2$). The charging and discharging paths of $L_B$ are connected in parallel. The polarity of transformer winding $N_1^*$ is such that the voltage across it is in opposition to the bulk voltage $V_B$ during the on-time of switch $S$, therefore, decreasing the voltage at node $X$. To obtain the same voltage at node $X$ during the on-time of switch $S$ as in the corresponding three-terminal cell in Fig. 1, the number of turns of winding $N_1^*$ should be

$$N_1^* = N_P - N_1. \tag{2}$$

where $N_1$ is the number of turns of winding $N_1$ in Fig. 1. The discharging path of $L_B$ in the two-terminal ICS cell in Fig. 9 is identical to the discharging path of $L_B$ in the corresponding three-terminal ICS cell in Fig. 1. Therefore, with $N_1^* = N_P - N_1$, the $S^2$ICS circuit with the two-terminal ICS cell in Fig. 9 is functionally equivalent to the $S^2$ICS circuit with the three-terminal ICS cell in Fig. 1.

Generally, for each $S^2$ICS circuit with a three-terminal ICS cell in Figs. 1–6, there exists a functionally equivalent $S^2$ICS circuit with a two-terminal ICS cell. The corresponding $S^2$ICS circuit with a two-terminal ICS cell to the $S^2$ICS circuit with the three-terminal ICS cell in Fig. 2 is presented in Fig. 10. It should be noted that the two-terminal ICS cell in Fig. 10 can be simplified for the case $N_1^* = N_2$, as shown in Fig. 11. The
Fig. 11. DCM $S^2ICS$ circuit with two-terminal ICS cell (Magnetic switch power supply) [2].

Fig. 12. $S^2ICS$ circuit with two-terminal inductive CCM-ICS cell [7].

Fig. 13. $S^2ICS$ circuit with two-terminal capacitive CCM-ICS cell [2].

Fig. 14. Generalized topology of $S^2ICS$ circuit with two-terminal ICS cell.

$S^2ICS$ circuit with the two-terminal ICS cell in Fig. 11 was first reported in [2] and called a magnetic switch (MS) power supply. For the $S^2ICS$ circuits with the three-terminal CCM-ICS cells in Figs. 3 and 4, the corresponding $S^2ICS$ circuits with two-terminal ICS cells are shown in Figs. 12 [7] and 13 [2], respectively. The $S^2ICS$ circuit with the generalized two-terminal ICS cell is shown in Fig. 14. Finally, possible new implementations of the two-terminal ICS cells, which correspond to the new implementations of the three-terminal ICS cells in Fig. 6, are shown in Fig. 15.

Generally, the $S^2ICS$ circuits with two-terminal and three-terminal ICS cells are functionally equivalent and, hence, they exhibit similar performance. Differences between them are mostly related to the transformer design. A $S^2ICS$ circuit with a two-terminal ICS cell requires at least one additional transformer winding (winding $N_4^*$ in Figs. 8–15) and, consequently, it may require a larger transformer than the corresponding $S^2ICS$ circuit with a three-terminal ICS cell if winding $N_1$ is implemented by tapping the primary winding of the transformer. It should be noted that the $S^2ICS$ circuits with three-terminal ICS cells are limited to single-ended topologies such as the single-switch forward and flyback converters. On the other hand, the $S^2ICS$ circuits with two-terminal ICS cells can be implemented with any isolated dc/dc converter such as the two-switch and the full-bridge forward converters.

III. EXPERIMENTAL RESULTS

To experimentally verify the conclusions in Section II, a pair of $S^2ICS$ circuits with three-terminal and two-terminal inductive CCM-ICS cells shown in Figs. 7 and 12, respectively, with a forward output was selected. The experimental $S^2ICS$ circuits were designed for a 200-W (5-V/40-A), 180–265-V$_{ms}$ line-voltage power supply. The major components of the circuit are as follows: $L_B = 408 \mu H$, $L_1 = 124 \mu H$, $TR$—EER35 core with $N_P = 49$ turns, $N_S = 3$ turns, $N_1 = 25$ turns, $N_4^* = 24$ turns, $C_B = 220 \mu F/450 V$, $S$—IXFH12N100, and secondary-side diodes—81CNQ045. The reset of the forward transformer was achieved with a reset winding. The switching frequency was 70 kHz. The control circuit was implemented using the low-cost integrated controller UC3825A.

Measured line-voltage and line-current waveforms at nominal line ($V_{in} = 230 V_{ms}$) and full load ($I_o = 40 A$) for both implementations are shown in Fig. 16. As can be seen, the line-current waveforms are almost identical. The corresponding line-current harmonics are shown in Fig. 17. The harmonic limits for the IEC 1000-3-2 Class D standard are also given in Fig. 17.
Both implementations satisfy the IEC 1000-3-2 Class D standard with enough margins. Comparative efficiency measurements at full load versus line voltage are presented in Fig. 18. The difference between the efficiencies of the two implementations is less than 0.5%. Finally, comparative bulk-voltage measurements at maximum line voltage \(V_{\text{in}} = 265 \, \text{V}_{\text{rms}}\) versus load current are presented in Fig. 19. For both implementations, the maximum bulk voltage is around 410 V which was obtained at a load current slightly below 10 A.

All the experimental results in Figs. 16–19 verify that the two implementations of the selected S\(^2\)ICS circuit with three-terminal and two-terminal inductive CCM-ICS cells exhibit only minor performance differences, which is the result of the slightly different transformer structure and, eventually, the measurement error.

**IV. SUMMARY**

Two generalized topologies of single-stage input-current-shaping (S\(^2\)ICS) circuits are presented: S\(^2\)ICS circuits with two-terminal ICS cells and S\(^2\)ICS circuits with three-terminal ICS cells. It was shown analytically and verified experimentally that the two generalized S\(^2\)ICS topologies are functionally equivalent.

**REFERENCES**


Laszlo Huber (M’86) was born in Novi Sad, Yugoslavia, in 1953. He received the Dipl.Eng. and Ph.D. degrees from the University of Novi Sad in 1977 and 1992, respectively, and the M.S. degree from the University of Niš, Niš, Yugoslavia, in 1983, all in electrical engineering.

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Dr. Lee received the Society of Automotive Engineering’s Ralph R. Teeter Education Award (1985), Virginia Tech’s Alumni Award for Research Excellence (1990), and its College of Engineering Dean’s Award for Excellence in Research (1997), the William E. Newell Power Electronics Award in 1989, the highest award presented by the IEEE Power Electronics Society for outstanding achievement in the power electronics discipline, the Power Conversion and Intelligent Motion Award for Leadership in Power Electronics Education (1990), the Arthur E. Fury Award for Leadership and Innovation in Advancing Power Electronic Systems Technology (1998), the IEEE Millennium Medal, and honorary professorships from Shanghai University of Technology, Shanghai Railroad and Technology Institute, Nanjing Aeronautical Institute, Zhejiang University, and Tsinghua University. He is an active member in the professional community of power electronics engineers. He chaired the 1995 International Conference on Power Electronics and Drives Systems, which took place in Singapore, and co-chaired the 1994 International Power Electronics and Motion Control Conference, held in Beijing. During 1993–1994, he served as President of the IEEE Power Electronics Society and, before that, as Program Chair and then Conference Chair of IEEE-sponsored power electronics specialist conferences.