

A New, Soft-Switched, High-Power-Factor Boost Converter With IGBTs

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Abstract—A new soft-switching technique that improves performance of the high-power-factor boost rectifier by reducing switching losses is introduced. The losses are reduced by an active snubber which consists of an inductor, a capacitor, a rectifier, and an auxiliary switch. Since the boost switch turns off with zero current, this technique is well suited for implementations with insulated-gate bipolar transistors. The reverse-recovery-related losses of the rectifier are also reduced by the snubber inductor which is connected in series with the boost switch and the boost rectifier. In addition, the auxiliary switch operates with zero-voltage switching. A complete design procedure and extensive performance evaluation of the proposed active snubber using a 1.2-kW high-power-factor boost rectifier operating from a $90 V_{\text{rms}}$ – $256 V_{\text{rms}}$ input are also presented.

Index Terms—Active snubber, boost converter, IGBT, power factor correction, reverse recovery loss, zero current switching, zero voltage switching.

I. INTRODUCTION

RECENTLY, several high-speed insulated-gate bipolar transistor (IGBT) families suitable for high-frequency switch-mode-power-supply applications have been introduced. Capable of operating at switching frequencies as high as 150 kHz and exhibiting a relatively small conduction loss at high currents, these IGBTs appear as a viable alternative to traditionally used metal-oxide-semiconductor field-effect transistors (MOSFETs) in many high-voltage, high-current applications such as boost input-current shapers. Nevertheless, to achieve efficient and reliable operation of an IGBT, it is necessary to ensure that the IGBT is switched under favorable switching conditions. Specifically, due to the IGBT's collector current "tail" effect during the turn-off, which increases the turn-off switching loss and limits the maximum switching frequency, the optimal performance of the IGBT can be achieved by turning-off the IGBT at zero current [1].

A zero-current-switching (ZCS) boost converter suitable for applications with IGBTs was introduced in [2]. Although in this circuit the boost switch is turned off at zero current, the circuit exhibits a strong undesirable resonance between the snubber inductor and the output capacitance of the switches, which requires additional clamp and/or snubber circuits [3].

In this paper, a soft-switching technique which is suitable for IGBT applications, and which does not suffer from undesirable resonances of circuit's components is proposed. The proposed

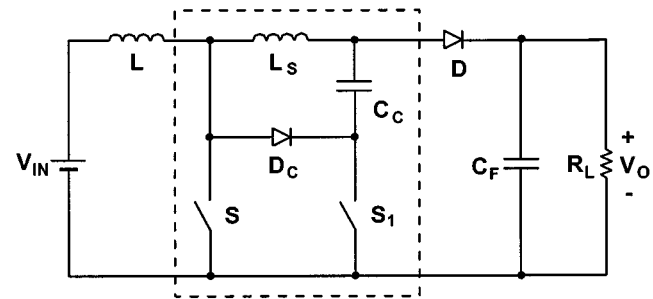


Fig. 1. Boost power stage with new ZC-ZVS active snubber.

technique improves the performance of the boost input-current shaper by eliminating the switching losses with a new zero-current-zero-voltage-switched (ZC-ZVS) active-snubber circuit that consists of a snubber inductor, a clamp diode, a clamp capacitor, and an auxiliary switch. The ZC-ZVS snubber reduces the reverse-recovery-related losses of the rectifier and also provides soft switching of the main and auxiliary switches. Specifically, the main switch turns off with ZCS, whereas the auxiliary switch turns on with ZVS. In addition, because the proper operation of the ZC-ZVS snubber requires that the conduction period of the main switch and the auxiliary switch overlap, the proposed boost converter with active snubber is not susceptible to failures due to accidental transient overlapping of the main and auxiliary switch gate drives. Moreover, the complexity and cost of the converters using the proposed technique is further reduced because the proposed ZC-ZVS active snubber requires a simple nonisolated (direct) gate drive for both switches.

Finally, a complete design procedure of the proposed soft-switched boost converter as well as extensive experimental evaluations of its performance are presented. The evaluation was performed on a single-phase, 1.2-kW, 80-kHz, high-power-factor boost rectifier operating in the universal line voltage range of $90 V_{\text{rms}}$ – $265 V_{\text{rms}}$.

II. ANALYSIS OF OPERATION

The circuit diagram of the boost converter that employs the new ZC-ZVS active snubber is shown in Fig. 1. The circuit in Fig. 1 uses snubber inductor L_S , which is connected in series with main switch S and rectifier D , to control the di/dt rate of the rectifier. Along with S , and L_S , auxiliary switch S_1 , clamp capacitor C_C , and clamp diode D_C form a ZC-ZVS active snubber as indicated by dashed lines in Fig. 1.

To simplify the analysis of operation, it is assumed that the inductance of boost inductor L is large so that it can be represented by constant-current source I_{IN} , and that the output-ripple

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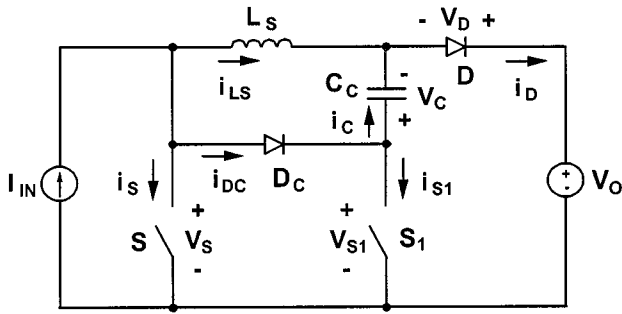


Fig. 2. Simplified circuit diagram of the proposed boost power stage showing reference directions of currents and voltages.

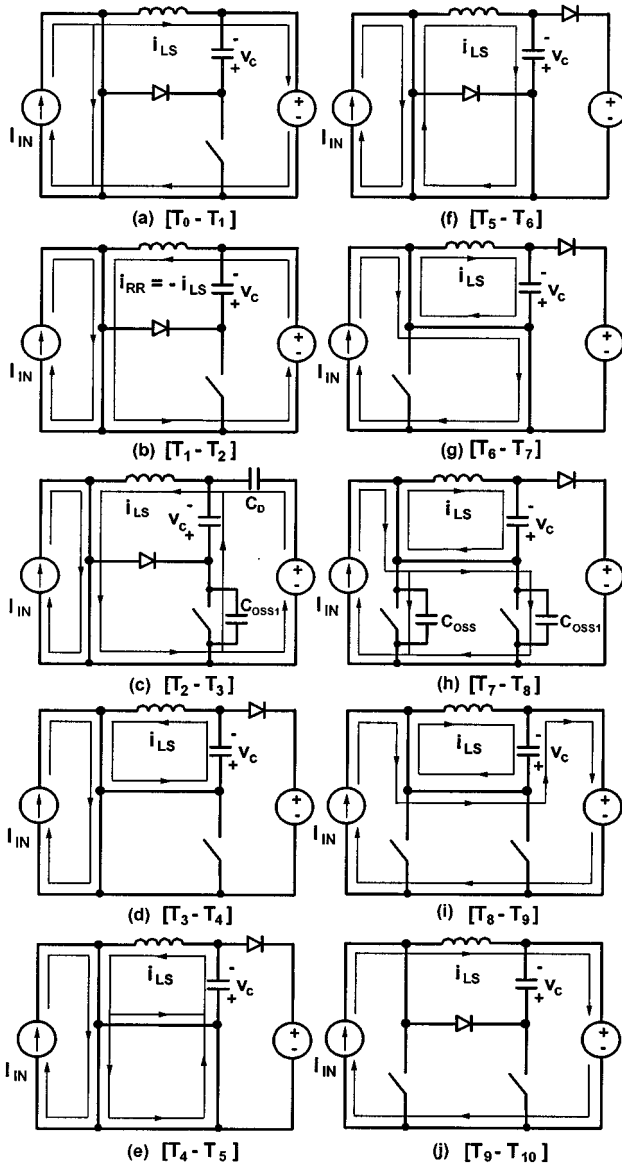


Fig. 3. Topological stages of the proposed boost power stage when the peak resonant current $I_{LS(PK)}$ is smaller than input current I_{IN} .

voltage is negligible so that the voltage across the output filter capacitor can be represented by constant-voltage source V_O . Also, it is assumed that in the on state, semiconductors exhibit

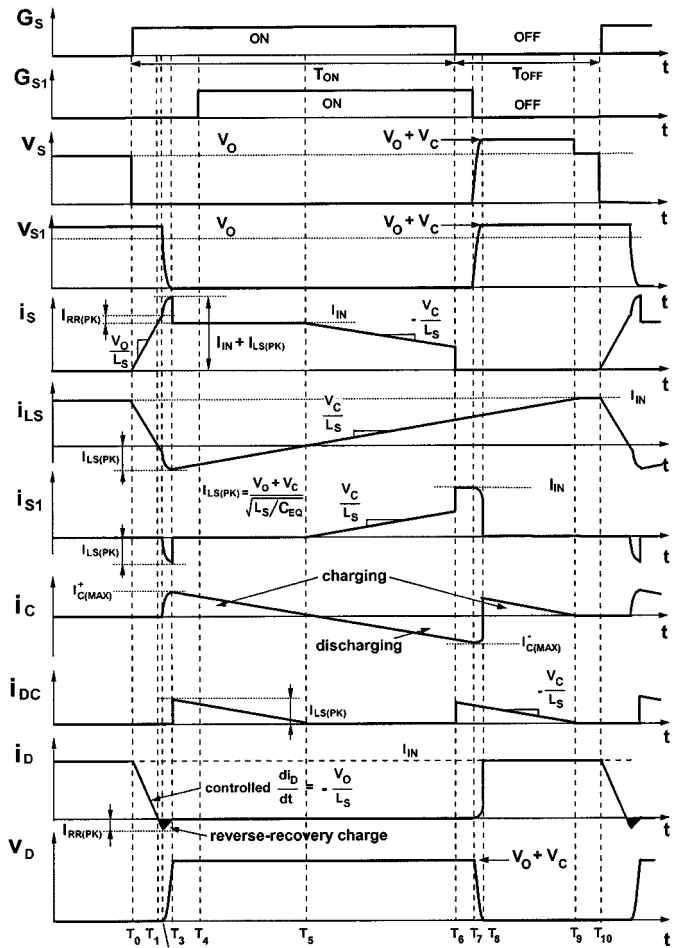


Fig. 4. Key waveforms of the proposed boost power stage when the peak resonant current $I_{LS(PK)}$ is smaller than input current I_{IN} .

zero resistance, *i.e.*, they are short circuits. However, the output capacitance of the switches and the reverse-recovery charge of the rectifier are not neglected in this analysis. The circuit diagram of the simplified converter is shown in Fig. 2.

To further facilitate the explanation of the operation, Fig. 3 shows topological stages of the circuit in Fig. 1 during a switching cycle, whereas Fig. 4 shows the power-stage key waveforms. As can be seen from the gate-drive timing diagrams for the boost and auxiliary switches in Fig. 4, the proposed circuit operates with an overlapping gate drive of the switches where the main switch turns on and off slightly prior to the auxiliary switch, *i.e.*, both switches conduct simultaneously during the major period of the on-time and share the current.

Before main switch S is turned on at $t = T_0$, the entire input current I_{IN} flows through snubber inductor L_S and boost rectifier D . At the same time, main switch S is off blocking output voltage V_O , whereas, auxiliary switch S_1 is off blocking a voltage which is the sum of output voltage V_O and clamp-capacitor voltage V_C , *i.e.*, $V_O + V_C$.

After switch S is turned on at $t = T_0$, a constant voltage V_O is applied across L_S , as shown in the equivalent circuit in Fig. 3(a). As a result, inductor current i_{LS} and rectifier current i_D decrease linearly, whereas switch current i_S increases at the

same rate. The rate of the rectifier current decrease is governed by

$$\frac{di_D}{dt} = -\frac{V_O}{L_S}. \quad (1)$$

Since the rate of the boost-rectifier-current decrease is controlled by snubber inductance L_S , the rectifier recovered charge and the associated losses can be reduced by a proper selection of the L_S inductance. Generally, a larger inductance, which gives a lower di_D/dt rate, results in a more efficient reduction of the reverse recovery-associated losses [4].

At $t = T_1$, when i_{LS} and i_D decrease to zero, the entire input current I_{IN} flows through switch S , as shown in Fig. 4. Ideally, when i_D falls to zero at $t = T_1$, rectifier D should stop conducting. However, due to a residual stored charge, reverse-recovery current i_{RR} will flow through rectifier D , as shown in Fig. 3(b). When, at $t = T_2$, the stored charge is recovered from the junction of rectifier D and the rectifier regains its blocking capability, a resonant circuit consisting of snubber inductor L_S , snubber capacitor C_C , output capacitor C_{OSS1} of auxiliary switch S_1 , and junction capacitor C_D of rectifier D is formed, as shown in Fig. 3(c). As a result, during the T_2 – T_3 interval, the drain voltage of auxiliary switch S_1 decreases from $V_O + V_C$ to zero in a resonant fashion. At $t = T_3$, when V_{S1} falls to zero, peak resonant current $I_{LS(PK)}$, which flows in the negative direction through L_S , is given by

$$I_{LS(PK)} = i_{LS}(t = T_3) = \frac{V_O + V_C}{\sqrt{\frac{L_S}{C_{EQ}}}} \quad (2)$$

where $C_{EQ} = C_{OSS1}C_C/(C_{OSS1} + C_C) + C_D \approx C_{OSS1} + C_D$ because for a properly designed circuit $C_C \gg C_{OSS1}$. From Fig. 3(c), the peak current of clamp capacitor C_C at $t = T_3$, $I_{C(MAX)}^+$, is

$$I_{C(MAX)}^+ = i_C(t = T_3) = \frac{C_{OSS1}}{C_{OSS1} + C_D} \times \frac{V_O + V_C}{\sqrt{\frac{L_S}{C_{EQ}}}}. \quad (3)$$

After the voltage across auxiliary switch S_1 falls to zero at $t = T_3$, clamp diode D_C starts conducting, as shown in Fig. 3(d). When D_C is conducting, clamp capacitor voltage V_C is applied across L_S and snubber-inductor current i_{LS} increases linearly, as illustrated in Fig. 4. If the capacitance of clamp capacitor C_C is large, capacitor voltage V_C is almost constant so that inductor current i_{LS} increases and capacitor current i_C decreases linearly, *i.e.*, $di_{LS}/dt = -di_C/dt = V_C/L_S$. Otherwise, i_{LS} and i_C change in a resonant fashion. This topological stage ends at $t = T_5$, when i_C reaches zero and clamp diode D_C stops conducting. As can be seen from Fig. 4, to achieve ZVS of auxiliary switch S_1 , it is necessary to turn on S_1 before $t = T_5$, *i.e.*, S_1 should be turned on while clamp diode D_C is conducting. In Fig. 4, auxiliary switch S_1 is turned on at $t = T_4$. It should be noted that after $t = T_4$, current i_{LS} or a part of it may continue flowing through S_1 depending on the relative values of on-impedances of S_1 and D_C , as shown in Fig. 3(e). Since auxiliary switch S_1 starts conducting after clamp diode D_C ceases

to conduct at $t = T_5$, auxiliary-switch current i_{S1} continues to increase linearly, as illustrated in Fig. 3(f). At the same time, main-switch current i_S decreases at the same rate because the sum of i_{S1} and i_S is equal to the constant input current I_{IN} .

When main switch S is turned off at $t = T_6$, the current which was flowing through switch S is diverted to auxiliary switch S_1 through clamp diode D_C as shown in Fig. 3(g). It should be noted that at the moment of switch S turn-off at $t = T_6$, the current of S is smaller than I_{IN} , as shown in Fig. 4. In addition, the voltage across switch S during its turn-off is clamped to zero by conducting clamp diode D_C and auxiliary switch S_1 , as can be seen from Fig. 3(g). As a result, switch S is turned off with a greatly reduced channel current and with zero voltage. In fact, the circuit can be designed to achieve complete ZCS of main switch S during the turn-off time, as it will be discussed later. During the T_6 – T_7 interval, input current I_{IN} flows through S_1 , whereas C_C continues to discharge through L_S . This interval ends at $t = T_7$ when auxiliary switch S_1 is turned off. It should be noted that auxiliary switch S_1 shares the input current with main switch S during the time interval between $t = T_5$ and $t = T_6$, as shown in Figs. 3(f) and 4. Therefore, by the addition of auxiliary switch S_1 , the overall rms current of main switch S is reduced.

After switch S_1 is turned off at $t = T_7$, current I_{IN} flowing through switch S_1 is diverted from the switch to its output capacitance C_{OSS1} , as shown in Fig. 3(h). As a result, the voltage across auxiliary switch S_1 starts to increase linearly from zero to $V_O + V_C$ due to the constant charging current I_{IN} . At the same time, because of conducting D_C , voltage V_S of main switch S also increases from zero toward $V_O + V_C$. When the voltage across switches S and S_1 reaches $V_O + V_C$ at $t = T_8$, rectifier D starts conducting, as shown in Fig. 3(i). During the T_8 – T_9 time interval, i_{LS} continues to increase toward I_{IN} , while clamp capacitor C_C is being charged by the difference of input current I_{IN} and snubber inductor current i_{LS} , *i.e.*, by $I_{IN} - i_{LS}$. When, at $t = T_9$, i_{LS} reaches I_{IN} , clamp diode D_C stops conducting and the entire input current flows through D , as shown in Fig. 3(j). The circuit stays in this topological stage until the next switching cycle is initiated at $t = T_{10}$.

At light load operation, when input current I_{IN} is smaller than the peak resonant current $I_{LS(PK)}$ described in (2), the charge balance of clamp capacitor C_C is completed during switch-on period. Figs. 5 and 6 show the power-stage operation when I_{IN} is smaller than $I_{LS(PK)}$. Fig. 5 shows topological stages during a switching cycle, whereas Fig. 6 shows the power-stage key waveforms.

During the T_0 – T_5 interval, the key waveforms and power-stage operation when I_{IN} is smaller than $I_{LS(PK)}$ are the same as in the case when I_{IN} is greater than $I_{LS(PK)}$, Figs. 3 and 4. However, after $t = T_5$, the operation when I_{IN} is smaller than $I_{LS(PK)}$ is different from that shown in Figs. 3 and 4. Since when I_{IN} is smaller than $I_{LS(PK)}$, snubber-inductor current i_{LS} reaches I_{IN} level before main switch S turned off at $t = T_6$, auxiliary switch S_1 carries the entire input current during the T_6 – T_8 interval as shown in Fig. 6. Therefore, to achieve a complete ZCS of the main switch, the peak resonant current $I_{LS(PK)}$ should be designed to be greater than input current I_{IN} over the entire load and line range.

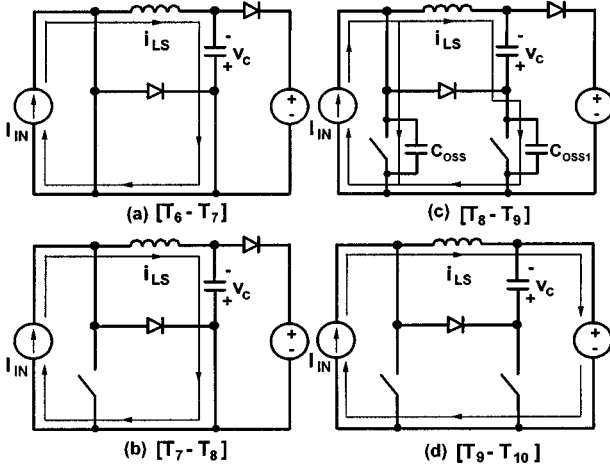


Fig. 5. Topological stages of the proposed boost power stage when I_{IN} is smaller than the peak resonant current $I_{LS(PK)}$.

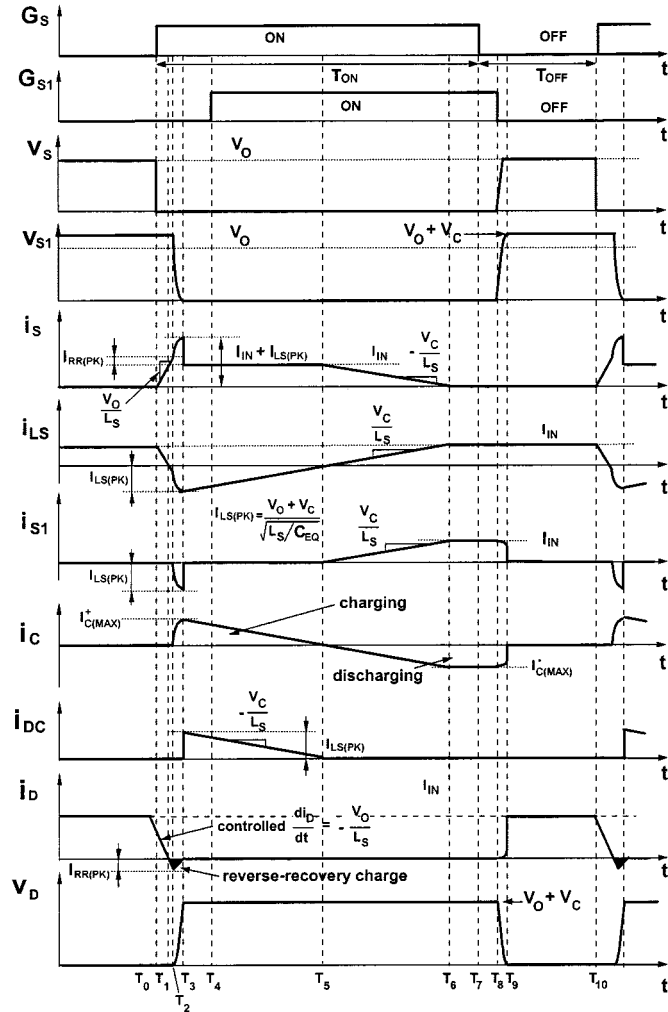


Fig. 6. Key waveforms of the proposed boost power stage when I_{IN} is smaller than the peak resonant current $I_{LS(PK)}$.

As can be seen from the waveforms in Fig. 4, to achieve a complete ZCS turn-off of main switch S , it is necessary that current through clamp capacitor i_C at the moment when S is turned off is equal to input current I_{IN} , *i.e.*

$$i_C(t = T_6) = I_{IN}. \quad (4)$$

Moreover, since for a properly designed circuit the T_6 – T_7 time interval is much shorter than the T_5 – T_6 time interval in Fig. 4, the value of clamp capacitor current i_C at $t = T_6$ and $t = T_7$ is approximately the same, *i.e.*

$$i_C(t = T_6) \approx i_C(t = T_7) = I_{C(MAX)}^- \quad (5)$$

where $I_{C(MAX)}^-$ is the maximum discharging current, as indicated on the i_C waveform in Fig. 4. From (4) and (5), the ZCS condition for S can be defined as

$$I_{C(MAX)}^- = I_{IN}. \quad (6)$$

Since for the circuit design wherein $I_{C(MAX)}^- = I_{IN}$, C_C charging occurs only during the T_2 – T_5 interval, *i.e.*, the charging interval T_8 – T_9 shown in Fig. 4 does not exist, the charge balance of C_C requires that

$$I_{C(MAX)}^+ = i_C(t = T_3) \approx I_{C(MAX)}^- \approx I_{IN}. \quad (7)$$

From (3) and (7), the ZCS condition can be written as

$$\frac{1}{C_{OSS1}} \sqrt{L_S(C_{OSS1} + C_D)} \leq \frac{V_O + V_C}{I_{IN}}. \quad (8)$$

If (8) is satisfied at the maximum power, *i.e.*, for $I_{IN} = I_{IN(MAX)}$, complete ZCS of switch S is achieved in the full load range. It should be noted that because auxiliary switch S_1 and rectifier D are both turned on under ZVS condition, external capacitance can be added across S_1 or D without incurring additional switching losses. If it is necessary to satisfy (8) for given V_O , $I_{IN(MAX)}$, L_S , V_C , and for given C_{OSS1} and C_D , external capacitance can be added in parallel with C_{OSS1} or C_D . However, since main switch S is always turned off with ZVS, the complete ZCS of main switch S is not necessary to improve overall performance of the converter. Therefore, the main switch current during turn-off (at $t = T_6$ in Fig. 4) needs to be optimized so that the peak resonant current $I_{LS(PK)}$ is not excessive.

As can be seen from Fig. 4, the voltage stress of main switch S , auxiliary switch S_1 , and rectifier D is $V_O + V_C$. Therefore, the voltage stress of main switch S in the proposed converter is higher compared to the corresponding stress in the conventional, “hard”-switched boost converter. To keep the voltage stress of switch S and switch S_1 within reasonable limits, it is necessary to select clamp-voltage level V_C properly.

The derivation of V_C dependence on the circuit parameters can be simplified by recognizing that in the boost converter in Fig. 1 that is designed to minimize the reverse-recovery-related losses and achieve complete ZCS of main switch S , the rectifier-current commutation interval T_0 – T_2 is much shorter than on-time period T_{ON} of switch S , and that capacitor charging period T_8 – T_9 is zero. In addition, the duration of the commutation periods T_2 – T_3 and T_7 – T_8 are negligible compared to the on-time interval of main switch S .

From Fig. 4, it can be seen that, from $t = T_3$ to $t = T_5$, clamp capacitor C_C is charged with current i_C which has a constant slope of $di_C/dt = V_C/L_S$. Therefore, since the circuit is designed to achieve ZCS of main switch S , $i_C(t = T_3) = I_{C(MAX)}^+ = I_{IN}$, and since the duration of the time interval from $t = T_2$ to $t = T_3$ is approximately one-half of the on-time of switch S , clamp-capacitor voltage V_C can be expressed as

$$V_C \approx L_S \frac{I_{IN}}{DT_S} = 2 \frac{L_S f_S I_{IN}}{D} \quad (9)$$

where D is the duty-cycle of switch S , T_S is the switching period, and f_S is the switching frequency. Since for a lossless boost power stage for which the current commutation interval T_0 – T_2 is much shorter than T_{ON} , the voltage-conversion ratio V_O/V_{IN} is given by

$$\frac{V_O}{V_{IN}} = \frac{I_{IN}}{I_O} = \frac{1}{1-D}. \quad (10)$$

Equation (10) can be written as

$$V_C \approx 2L_S f_S I_O \left(\frac{V_O^2}{(V_O - V_{IN}) V_{IN}} \right). \quad (11)$$

According to (11), V_C is maximum at full load $I_{O(MAX)}$ and high line $V_{IN(MAX)}$. For given input and output specifications, *i.e.*, for given $I_{O(MAX)}$, $V_{IN(MAX)}$, and V_O , clamp-capacitor voltage V_C can be minimized by minimizing the $L_S f_S$ product.

It should be noted that the control of the proposed boost converter can be implemented in the same way as in its conventional “hard” switched counterpart as long as an additional gate-drive circuit is provided. Specifically, in the input-current-shaping applications, the proposed converter can be implemented with any known control technique, such as average current, peak current, or hysteretic control.

III. DESIGN OF A 1.2-KW, HPF BOOST RECTIFIER PROTOTYPE

A 1.2-kW, HPF boost experimental rectifier was designed for the following specifications.

Input

- Voltage V_{IN} : 1-phase, 90 V_{RMS}–265V_{RMS}.
- Line Frequency f_L : 47–63 Hz.
- THD: <5%
- Power Factor: >0.99 (100% load).

Output

- Voltage V_O : 400 V_{dc}.
- Power P_O : 1.2 kW.
- Ripple Voltage: <6.5 V_{peak-peak} (100/120 Hz).
- Switch Frequency f_S : 80 kHz.

A. Design of Active Snubber Circuit

The analysis of the proposed soft-switching technique described in Section II can be applied to ac/dc PFC boost rectifiers. Since the switching frequency is much higher than the line frequency, the rectified ac input voltage of the boost rectifier is approximately constant during a switching cycle, and can be approximated as a dc voltage source.

To reduce the reverse-recovery-related losses, the di_D/dt rate of the majority of fast-recovery rectifiers should be kept below approximately 100 A/ μ s [4]. Generally, slower rectifiers require slower di_D/dt rates than faster rectifiers to achieve the same level of reduction of the reverse-recovery-related losses. As a rule of thumb, the practical range of snubber inductance L_S is from 2 μ H to 20 μ H. In fact, without a snubber, the rate of rectifier-current change is mainly decided by the parasitic inductance of the trace between boost switch S and rectifier D , which is generally less than several hundreds nanohenrys. As a result, the rate of rectifier-current change of the boost rectifier without a snubber inductor is approximately 2000 A/ μ s ($V_O/L_P = 400/0.2 \times 10^{-6}$). To reduce the stored charge which is directly

proportional to the reverse-recovery-related losses, snubber inductor L_S must be added.

Generally, the maximum value of snubber inductance L_S is limited by the voltage stress on switch S and auxiliary switch S_1 . As can be seen from Figs. 2 and 4, the voltage stress of switches S and S_1 are the same and equal to $V_O + V_C$. During the period when clamp diode D_C is not conducting, auxiliary switch S_1 blocks the voltage which is the summation of the clamp capacitor voltage and the output voltage. Boost switch S blocks the same voltage when clamp diode D_C is conducting. Compared to the corresponding stress in the conventional, “hard”-switched boost converter, the voltage stress of boost switch S in the proposed converter is higher for the amount of clamp voltage V_C . To keep the voltage stress of switches S and S_1 within reasonable limits, it is necessary to properly select clamp-voltage level V_C . Clamp-capacitor voltage V_C can be calculated by using (11). According to (11), V_C is the maximum at full load $I_{O(MAX)}$ and high line $V_{IN(MAX)}$, since switching frequency f_S and output voltage V_O are constant. For given input and output specifications, *i.e.*, for given $I_{O(MAX)}$, $V_{IN(MAX)}$, f_S , and V_O , the voltage stresses on the main and auxiliary switches can be minimized by minimizing snubber inductor L_S . From the specifications, the maximum input voltage $V_{IN(MAX)} = 375$ V, the maximum output current $I_{O(MAX)} = 3$ A, switching frequency $f_S = 80$ kHz, and output voltage $V_O = 400$ V. To reduce di_D/dt rate the value of snubber inductor L_S was chosen to be approximately 3.3 μ H. This value results in $di_D/dt = 120$ A/ μ s and $V_C = 27$ V. The maximum voltage stress of the switch is below 427 V which is quite acceptable even for a 500-V rated device.

Since the average voltage across the clamp-capacitor is independent from the size of the clamp capacitor C_C as shown in (11), the value of C_C can be selected to minimize the switch-frequency voltage ripple. Since the energy stored in the snubber inductor contributes to the voltage ripple during a switching cycle, the maximum switch-frequency voltage ripple $V_{C(P-P)}$ can be expressed as

$$V_{C(P-P)} = I_{O(max)} \sqrt{\frac{L_S}{C_C}}. \quad (12)$$

The choice of two 6.8 μ F/100 V ceramic capacitors in parallel for the clamp capacitor limits the magnitude of the maximum peak-to-peak ripple voltage to approximately 1.5 V, which is less than 20% of V_C over the entire input voltage and load range.

B. Selection of Components

Semiconductors: The peak voltage stress on switch S is approximately 430 V as explained in Section III-A. The peak current stress on S , which is equal to the peak input current is approximately $I_{IN(MAX)} = \sqrt{2}P_O/(\eta \times PF \times V_{IN}) = \sqrt{2} \times 1200/(0.92 \times 0.99 \times 90) \cong 21$ A at full load and low line. An IXGK 50N60B IGBT from IXYS ($V_{CES} = 600$ V, $I_{C90} = 50$ A, $V_F = 2.5$ V) is used for boost switch S . The peak voltage stress on auxiliary switch S_1 is the same as that of switch S . Also, the peak current stress on S_1 is equal to the peak current stress of S , *i.e.*, it is equal to the input current at full load and low line. However, the average current of S_1 ,

$\langle i_{S1} \rangle$, is much smaller than the average current of S , $\langle i_S \rangle$, as can be seen from Fig. 4. As a result, a smaller IGBT can be selected for S_1 . In the experimental circuit, an HGTG 20N60B3 IGBT from Harris ($V_{CES} = 600$ V, $I_{C110} = 20$ A, $V_F = 2$ V) is used for S_1 . Although S_1 turns on with ZVS and can be implemented with a MOSFET device, in the experimental circuit an IGBT is also used for auxiliary switch S_1 together with boost switch S . To reduce the turn-off switching loss of S_1 and optimize the peak value of snubber-inductor current $I_{LS(PK)}$, capacitor C_P (200 pF/1 kV) is connected in parallel with S_1 . Specifically, the value of capacitor C_P is chosen so that $I_{LS(PK)}$ is approximately equal to input current I_{IN} , in order to achieve ZCS turn-off of S , as seen in Fig. 4. Generally, the output capacitance of a similarly rated MOSFET switch is approximately five times larger than that of a IGBT switch. As a result, an additional capacitor is not required when a MOSFET switch is utilized for S_1 .

Since, output diode D has the same voltage stress as that of switch S and must conduct a maximum load current of 3 A, two RHRP3060 diodes from Harris ($V_{RRM} = 600$ V, $I_{FAVM} = 30$ A, $t_{rr} = 40$ ns) connected in parallel were used for output diode D . To reduce the conduction loss of the output diode, the devices which have a significantly higher current rating than the maximum current were selected. The voltage stress of clamp diode D_C is the same as that of output diode D . However, since the circulating current through $L_S - D_C$ loop is small, a RHRP3060 diode is used for D_C .

Boost Inductor: Since the desired inductance of boost inductor L is 0.5 mH, four 0.125 mH inductors are built using a toroidal core (Magnetics, Kool- μ 77 071-A7) and 45 turns of magnet wire (AWG #12). Four small-size cores are used to reduce the overall height of the power supply.

Snubber Inductor: Snubber inductor $L_S = 3.3 \mu\text{H}$ was built using a toroidal core (Magnetics, Kool- μ 77 312-A7) and 12 turns of magnet wire (AWG #12).

Clamp Capacitor: Two 6.8 μF , 100 VDC, ceramic capacitors connected in parallel are used for clamp capacitor C_C to limit the magnitude of the maximum peak-to-peak ripple voltage to approximately 1.5 V. Since the peak clamping capacitor voltage is approximately 30 V for this prototype, 100 VDC ceramic capacitors are utilized.

IV. EVALUATION

The component values of the experimental circuit power stage are shown in Fig. 7. The control circuit was implemented with the average-current PFC controller UC3854. The TC427 driver is used to generate the required gate-drive signal for the main switch and the auxiliary switch. The value of resistor R_D is selected large enough so that it doesn't affect normal circuit operation. Resistor R_D is added to discharge capacitor C_C when the PFC boost rectifier is no longer operating.

Fig. 8 shows the oscillograms of key waveforms of the experimental converter with the IGBT implementation at the low line and full power. The oscillograms in Fig. 8 is taken at the peak of the line current, i.e., when the duty cycle is at the minimum. As can be seen comparing corresponding waveforms in Figs. 4 and 8, there is a good agreement between the experimental and

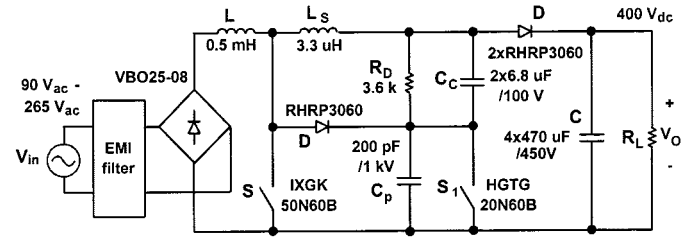


Fig. 7. Experimental 1.2 kW, boost power stage with a ZC-ZVS active snubber.

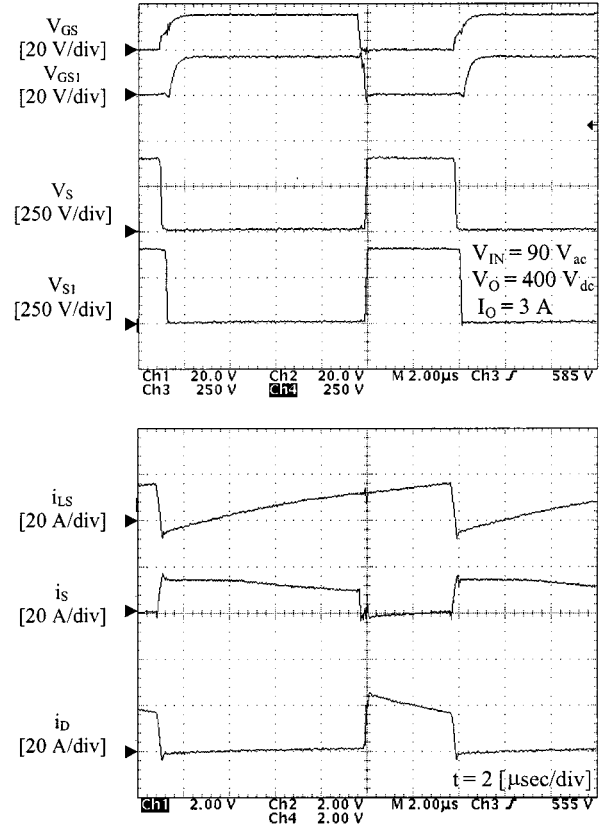


Fig. 8. Measured key waveforms of experimental converter at $P_O = 1.2$ kW and $V_{IN} = 90$ V_{rms}. Time base: 2 $\mu\text{s}/\text{div}$.

theoretical waveforms. As can be seen from Fig. 8, auxiliary switch S_1 is turned on with ZVS since its voltage V_{S1} falls to zero before gate-drive signal V_{GS1} becomes high. However, boost switch S is turned on while voltage across it is equal to output voltage $V_O = 400$ V. Despite this “hard” turn on of boost switch S , all waveforms are free from parasitic ringing, since the output capacitance of IGBTs is much smaller than that of MOSFETs. In fact, since the overall switching loss of IGBTs is dominated by its turn-off loss due to the current tailing effect, the optimum switching strategy of IGBT is soft turn off, rather than soft turn on. As shown in Figs. 8 and 9, when switch S is turned off, switch current i_S is small and drain to source voltage V_S is clamped to zero until switch S_1 is turned off. Therefore, the turn-off loss of switches is very much reduced. Also, it should be noted that the boost-rectifier-current turn-off rate, which is controlled by L_S , is approximately $di_D/dt = 120$ A/ μs , as indicated in Fig. 8. With this di_D/dt rate, peak reverse-recovery

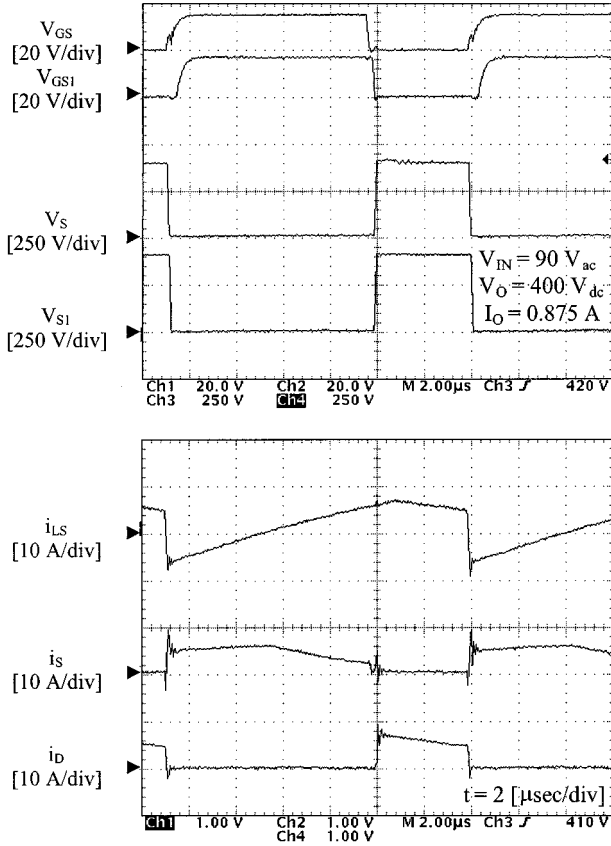


Fig. 9. Measured key waveforms of experimental converter at $P_O = 350$ W and $V_{IN} = 90$ V_{ac}. Time base: 2 μ s/div.

current I_{RR} is reduced to approximately 4 A, which corresponds to a recovered charge of approximately 100 nC.

The key waveforms of the experimental prototype at light load operation is shown in Fig. 9. When input current I_{IN} is smaller than the peak resonant current $I_{LS(PK)}$, the charge balance of clamp capacitor C_C is completed during the switch-on period as shown in Fig. 9.

Figs. 10 and 11 show the measured waveforms of the input line current and clamp capacitor voltage V_C of the prototype rectifier delivering 1.2 kW at 90 V and 265 V input voltages, respectively. Since the maximum duty cycle is not limited by the addition of the active snubber circuit, the input current waveforms with and without the active snubber circuit are nearly identical. The power factor of the prototype circuit measured at 90 V and 265 V input voltages are 99.3% and 98.4%, respectively.

Fig. 12 shows the measured efficiencies of the experimental converter with and without the active snubber at the minimum and maximum line voltages as functions of the output power. As can be seen from Fig. 12, for both line voltages the active snubber improves the conversion efficiency in the entire measured power range (200 W to 1.2 kW). Nevertheless, the efficiency improvement is more pronounced at the minimum line and higher power levels where the reverse-recovery losses are greater. Specifically, at the maximum line (265 V_{rms}), the efficiency improvement at 1.2 kW is 0.9%. However, at the minimum line, the implementation without the active snubber cannot deliver more than approximately 900 W due

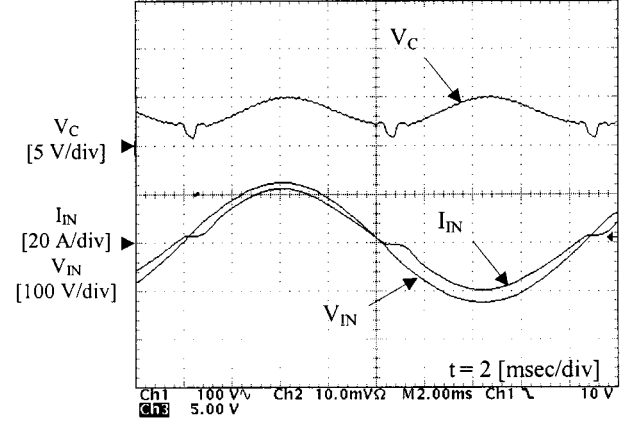


Fig. 10. Measured clamp capacitor voltage V_C , input current I_{IN} , and input voltage V_{IN} waveforms of experimental converter at $P_O = 1.2$ kW and $V_{IN} = 90$ V_{ac}. Time base: 2 msec/div.

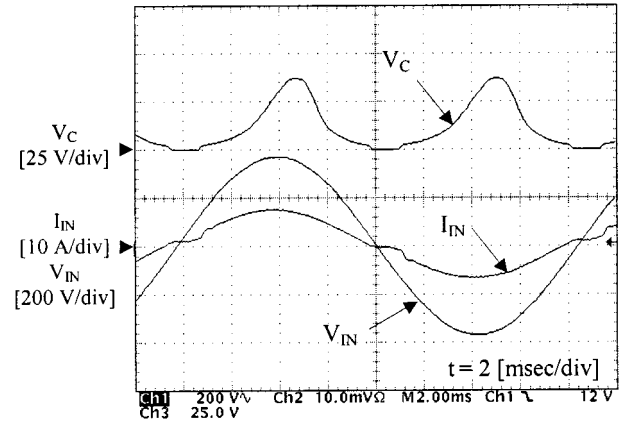


Fig. 11. Measured clamp capacitor voltage V_C , input current I_{IN} , and input voltage V_{IN} waveforms of experimental converter at $P_O = 1.2$ kW and $V_{IN} = 265$ V_{ac}. Time base: 2 msec/div.

to the thermal runaway of the switch caused by the excessive reverse-recovery losses. Even at $P_O = 900$ W, the active snubber improves the efficiency by approximately 3.4%, which translates into approximately 30% reduction of the losses.

Fig. 13 shows the measured temperatures of the experimental converter with and without the active snubber at the minimum line voltage as functions of the output power. The ambient temperature was approximately 26°C during the measurements. As can be seen from Fig. 13, at the same power levels, the temperatures of the semiconductor components in the implementation with the active snubber are significantly lower than those in the implementation without the snubber. As indicated in Figs. 12 and 13, at the maximum line (265 V_{rms}) and full power (1.2 kW), the case temperatures of the boost rectifier and boost switch in the implementation with the snubber are $T_d = 37^\circ\text{C}$ and $T_S = 35^\circ\text{C}$, respectively, whereas the corresponding temperatures in the implementation without the snubber are $T_d = 41^\circ\text{C}$ and $T_S = 39^\circ\text{C}$. Similarly, at the minimum line voltage (90 V_{rms}) and full power, the rectifier and switch temperatures in the implementation with the snubber are $T_d = 41^\circ\text{C}$ and $T_S = 86^\circ\text{C}$. As can be seen from Figs. 12 and 13, the implementation without the snubber cannot deliver the full power of 1.2 kW at the minimum line because

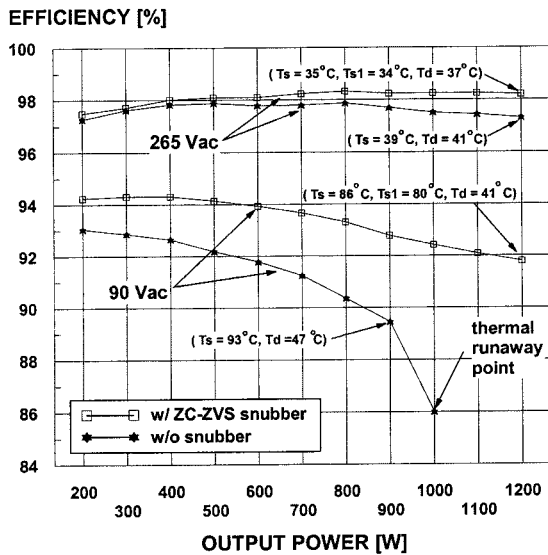


Fig. 12. Measured efficiencies of the experimental converter with and without ZC-ZVS active snubber at the minimum and maximum line voltages as functions of the output power. Note that the maximum possible output power for the implementation without the snubber is limited to 900 W.

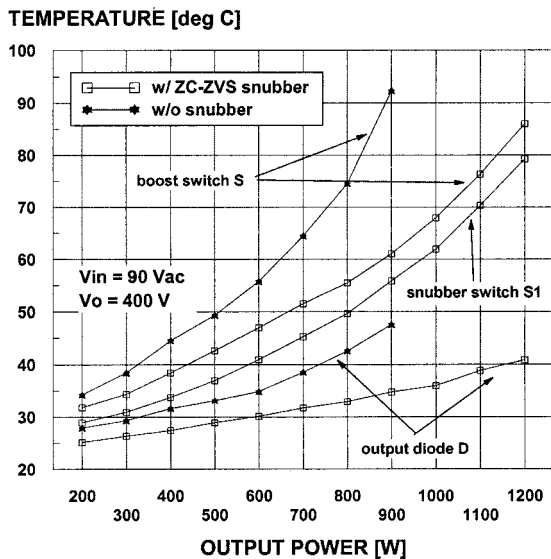


Fig. 13. Measured switch temperature of the experimental converter with and without ZC-ZVS active snubber at the minimum line voltage as functions of the output power.

the rectifier becomes thermally unstable at approximately 900 W. In fact, for the implementation without the snubber the temperature of the boost switch is $T_S = 93^\circ\text{C}$ at 900 W, which is significantly higher than the temperature of the switches ($T_S = 61^\circ\text{C}$, $T_{S1} = 56^\circ\text{C}$) in the implementation with the snubber at the same output power.

V. CONCLUSION

An active-snubber technique which reduces the reverse-recovery-related losses of the rectifier and also provides lossless switching for the main and auxiliary switches is described. A complete design procedure of a boost input-current shaper with the proposed active snubber is presented. Also, performance

evaluations on a 1.2-kW high-power-factor boost rectifier for server applications are given. It is shown that the proposed active-snubber technique can significantly extend the maximum power range at which a fast-recovery rectifier can be reliably employed.

REFERENCES

- [1] K. Wang, F. C. Lee, G. Hua, and D. Borjović, "A comparative study of switching losses of IGBTs under hard-switching, zero-voltage-switching, and zero-current-switching," in *Proc. IEEE Power Electron. Spec. Conf. (PESC) Rec.*, June 1994, pp. 1196–1204.
- [2] G. Hua, X. Yang, Y. Jiang, and F. C. Lee, "Novel zero-current-transition PWM converters," in *Proc. IEEE Power Electron. Spec. Conf. (PESC) Rec.*, June 1993, pp. 538–544.
- [3] K. Wang, G. Hua, and F. C. Lee, "Analysis, design and experimental results of ZCS-PWM boost converters," in *Proc. Int. Power Electron. Conf. Proc.*, Yokohama, Japan, Apr. 1995, pp. 1202–1207.
- [4] Y. Khersonsky, M. Robinson, and D. Gutierrez, "New fast recovery diode technology cuts circuit losses, improves reliability," *Power Conv. Intell. Motion (PCIM) Mag.*, pp. 16–25, May 1992.



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