

A New Family of Full-Bridge ZVS Converters

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Abstract—A family of soft-switched, full-bridge (FB) pulse-width-modulated (PWM) converters that feature zero-voltage-switching (ZVS) of all bridge switches over a wide range of input voltage and output load with minimal duty cycle loss and circulating current is described. The ZVS of primary switches is achieved by employing two magnetic components whose volt-second products change in the opposite directions with a change of phase shift between the two bridge legs. One magnetic component is a transformer while the other magnetic component is either a coupled inductor or a single-winding inductor. The transformer is used to provide isolated output(s), whereas the inductor is used to store energy for ZVS.

Index Terms—Constant-frequency, coupled inductor, full-bridge, phase shift, zero voltage switching.

I. INTRODUCTION

THE FULL-BRIDGE zero-voltage-switching pulse-width-modulated (FB ZVS-PWM) converter shown in Fig. 1 is the most widely used soft-switched circuit in high-power applications, [1]–[7]. This constant-frequency converter employs phase-shift control and features ZVS of primary switches with a relatively small circulating energy. However, full ZVS operation can only be achieved in a limited load and input-voltage range, unless a relatively large inductance is provided in series with the primary winding of the transformer which can be implemented by increasing leakage inductance of the transformer and/or adding an external inductor. This increased inductance has a detrimental effect on the performance of the converter since it causes an increased loss of duty cycle on the secondary side [as shown by the shaded area in Fig. 1(b)] as well as severe voltage ringing across the secondary-side output rectifiers, which is due to the resonance between the inductance and the junction capacitance of the rectifier.

Several techniques have been proposed to extend the ZVS range of FB ZVS converters without loss of duty cycle and secondary-side ringing [8]–[11]. Generally, these circuits achieve ZVS in all primary switches over an extended load and input-voltage range by utilizing energy stored in the inductive components of an auxiliary circuit. In the approach described and analyzed in [8] and [9], the auxiliary circuit comprises a pair of inductors that are connected between the mid-point of the bridge legs and the mid-point of an input-voltage capacitive divider, whereas in the approach described in [10], the auxiliary circuit comprises a pair of switches and an extra inductor. In the

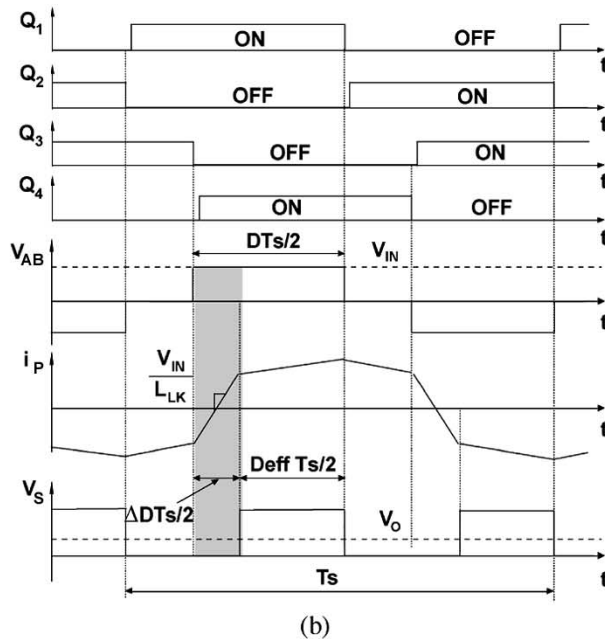
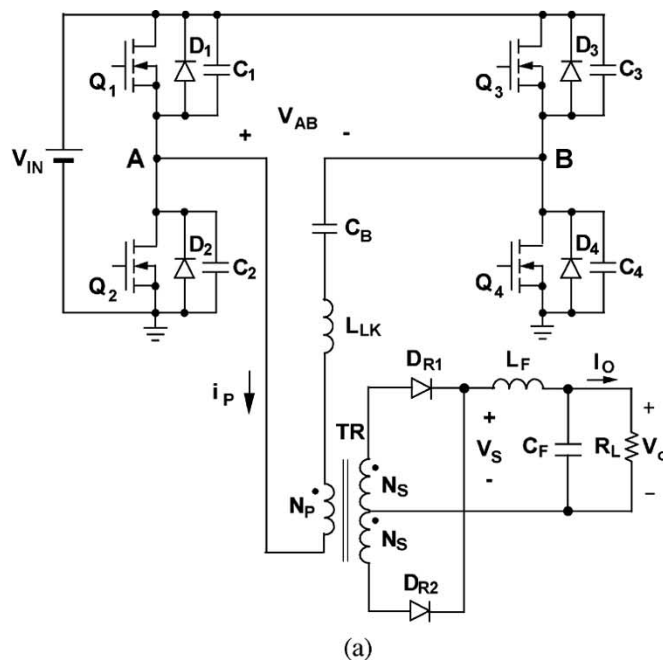


Fig. 1. Conventional FB ZVS-PWM converter and its key waveforms.

approach described in [11], the energy stored in the magnetizing inductance of the auxiliary transformer is used to extend the ZVS range. In the proposed FB ZVS-PWM converters, the energy available for ZVS increases as the input voltage increases, which is the desirable direction of change since more energy is required to achieve ZVS at higher input voltages. The stored energy in the proposed FB ZVS converters is independent of load.

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As a result, the proposed FB ZVS-PWM converters cannot optimally resolve the trade-off between power-loss savings brought about by a full-load-range ZVS and power losses of the auxiliary circuit. Ideally, the auxiliary circuit needs to provide very little energy, if any, at full load because the full-load current stores enough energy in converter's inductive components to achieve a complete ZVS for all switches. As the load current decreases, the auxiliary circuit needs to provide progressively more ZVS energy, with the maximum energy required at no load. A FB ZVS-PWM converter that features this kind of adaptive energy storage in the auxiliary circuit has been introduced in [12]. The circuit implements adaptive energy storage using a coupled inductor connected between its bridge legs.

In this paper, the concept introduced in [12] is generalized. The generalized FB ZVS-PWM circuit is then used to derive a family of FB ZVS-PWM converters that achieve a full-range ZVS with virtually no secondary-side duty-cycle loss and parasitic ringing.

II. NEW FAMILY OF FB ZVS-PWM CONVERTERS

Fig. 2 shows a generalized, isolated, phase-shift-controlled FB ZVS-PWM converter. The circuit in Fig. 2 employs two transformers T_X and T_Y that have their respective secondary outputs connected to two output circuits X and Y. In dc-dc implementations, each output circuit includes a rectifier, low-pass filter, and load. Two constant voltage sources V_1 and V_2 , connected in series with the primary winding of transformer T_X , are employed to provide a volt-second balance on the windings of both transformers so that the transformers do not saturate.

Generally, the volt-second products of the windings of transformers X and Y shown in Fig. 2 are dependent on the phase shift between the turn-on instances of the corresponding switches in bridge legs S_1 - S_2 and S_3 - S_4 , as illustrated in Fig. 3. Namely, for zero phase shift, i.e., when switches S_1 and S_2 and their corresponding switches S_3 and S_4 are turned on and off in unison ($D = 0$ in Fig. 3), voltage v_{AB} across the primary of transformer T_X is zero so that the volt-second product of the primary winding of transformer T_X is also zero. At the same time, since voltage v_{AC} across winding AC and voltage v_{CB} across winding CB must have equal polarity and since $v_{AB} = v_{AC} + v_{CB} = 0$, it follows that $v_{AC} = v_{CB} = 0$. As a result, voltage v_{CO} across the primary winding of transformer T_Y is $V_{IN}/2$, i.e., the volt-second product of the primary winding of transformer T_Y is maximal. Similarly, when switches S_1 and S_2 and their corresponding switches S_3 and S_4 are turned on and off in antiphase, i.e., with a 180° phase shift ($D = 1$ in Fig. 3), the volt-second product on the primary of transformer T_X is maximal, whereas the volt-second product of the primary winding of transformer T_Y is zero (minimal). Because the output voltages of output circuits X and Y are directly proportional to the volt-second products of the corresponding primary windings, the circuit in Fig. 2 delivers power to outputs X and Y in a complementary fashion. Specifically, for zero phase shift ($D = 0$), maximum power is delivered to output Y, whereas no power (or minimal power) is delivered to output X. For 180° phase shift ($D = 1$),

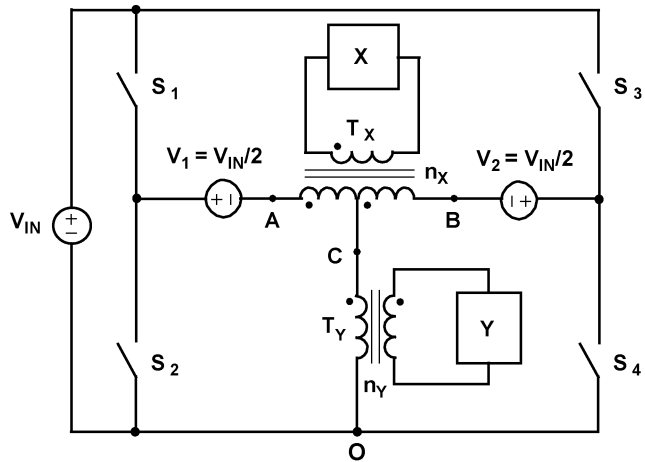


Fig. 2. Generalized FB ZVS-PWM converter.

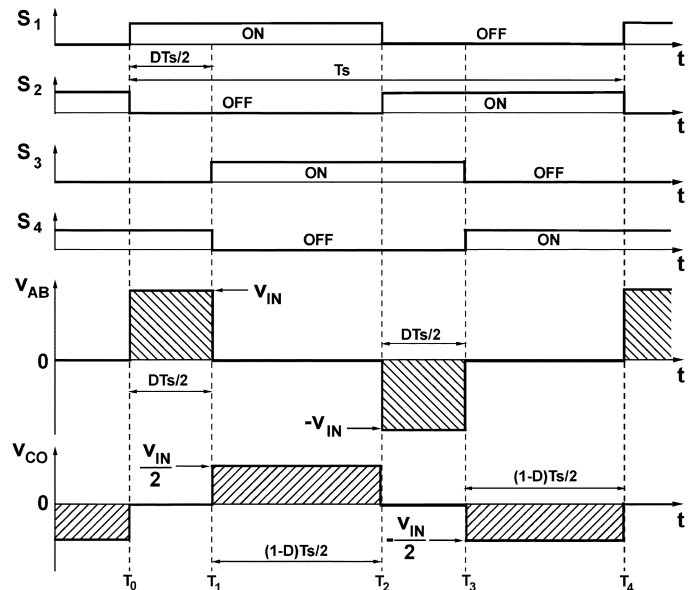


Fig. 3. Control timing diagrams of switches and voltages across primary windings of transformers T_X and T_Y (voltages v_{AB} and v_{CO} , respectively).

maximum power is delivered to output X, whereas no power is delivered to output Y.

Because the incremental changes of the delivered power to outputs X and Y with phase-shift changes are in opposite directions, the circuit in Fig. 2 cannot simultaneously regulate both outputs if constant-frequency control is employed. Nevertheless, the property of the circuit to deliver power to outputs X and Y in the complementary fashion makes the circuit ideal for implementing ZVS of the primary switches in a wide range of input voltage and load current. Namely, if in the converter in Fig. 2 one output is regulated, the energy in that output's filter inductor will decrease as the load decreases. At the same time, the energy stored in the magnetizing inductance of the corresponding transformer will also decrease because a lighter load requires a smaller volt-second product on the primary winding of the transformer. However, the filter-inductor energy in the other unregulated output circuit and in the magnetizing inductance of the corresponding transformer will increase because of

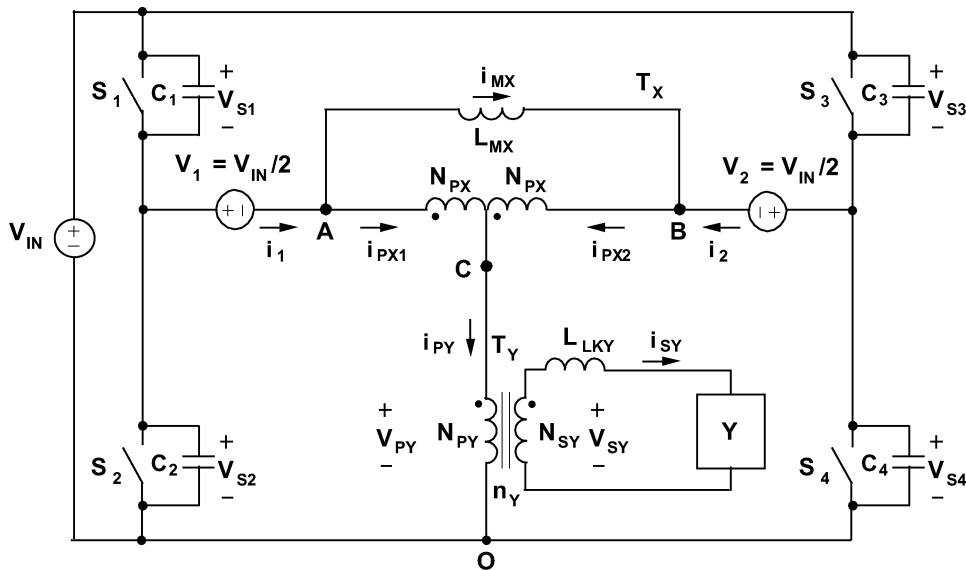


Fig. 4. Simplified circuit diagram of converter in Fig. 2 when output Y is regulated.

an increased volt-second product on the primary of the transformer. This increased energy in the output-filter inductor of the unregulated output and in the magnetizing inductance of its transformer can be used to create the ZVS condition for the primary switches at lighter loads, including no load.

To facilitate the analysis of the operation of the circuit in Fig. 2, Fig. 4 shows its simplified circuit diagram when output Y is regulated. In the simplified circuit in Fig. 4, it is assumed that only energy stored in the magnetizing inductance of transformer T_X is used to create the ZVS condition. Because no energy stored in the output filter inductor of output circuit X is used to create the ZVS condition, output circuit X and the associated secondary of transformer X are not shown in Fig. 4. Generally, this simplification does not have a significant effect on the operation of the circuit since the only effect of output circuit X is to increase the total available energy that can be used for creating the ZVS condition. However, due to a reduced component count, the implementation in Fig. 4 is preferred in practice. Because only the primary windings of transformer T_X are used in the circuit in Fig. 4, transformer T_X operates as a coupled inductor.

To further simplify the analysis, it is assumed that the resistance of the conducting semiconductor switches is zero, whereas the resistance of the nonconducting switches is infinite. In addition, the leakage inductances of transformer T_X and the magnetizing inductance of transformer T_Y are neglected since their effect on the operation of the circuit is not significant. However, the magnetizing inductance of transformer T_X , which operates as a coupled inductor, and the output capacitances of primary switches C_1 – C_4 are not neglected in this analysis because they play a major role in the operation of the circuit. Also, it should be noted that although the circuit in Fig. 4 does not rely on the energy stored in the leakage inductance of transformer T_Y to create conditions for ZVS and, therefore, the leakage inductance can be minimized, this minimized leakage inductance of T_Y is not neglected in this analysis since it has a profound effect on the shape of primary-side currents, as

described in [12, p. 235]. Consequently, in Fig. 4, transformer T_X is modeled as an ideal transformer with magnetizing inductance L_{MX} connected across the series connection of primary windings, whereas transformer T_Y is modeled by an ideal transformer with turns ratio n_Y and leakage inductance L_{LKY} connected in series with the secondary winding. It should be noted that magnetizing inductance L_{MX} of transformer T_X represents the inductance measured between terminals A and B.

With reference to Fig. 4, the following relationships between currents can be established:

$$i_{PY} = i_{PX1} + i_{PX2} \quad (1)$$

$$N_{PY}i_{PY} = N_{SY}i_{SY} \quad (2)$$

$$i_1 = i_{PX1} + i_{MX} \quad (3)$$

$$i_2 = i_{PX2} - i_{MX}. \quad (4)$$

Since the number of turns of winding AC and winding CB of transformer T_X are the same, it must be that

$$i_{PX1} = i_{PX2}. \quad (5)$$

Substituting (5) into (1)–(4) gives

$$i_{PX1} = i_{PX2} = \frac{i_{SY}}{2n_Y} \quad (6)$$

$$i_1 = \frac{i_{SY}}{2n_Y} + i_{MX} \quad (7)$$

$$i_2 = \frac{i_{SY}}{2n_Y} - i_{MX} \quad (8)$$

where $n_Y = N_{PY}/N_{SY}$ is the turns ratio of transformer T_Y .

As can be seen from (7) and (8), currents of both bridge legs i_1 and i_2 are composed of two components: load-current component $i_{SY}/2n_Y$ and magnetizing-current component i_{MX} . The load-current component is directly dependent on the load current, whereas the magnetizing current does not directly depend on the load but rather on the volt-second product across the magnetizing inductance. Namely, a change of the magnetizing current occurs only if the phase shift is changed to maintain

the output regulation. Generally, a change of phase shift with a load change is greater at lighter loads than at heavier loads because as the load decreases toward no load the converter enters discontinuous conduction mode. Since the phase shift increases as the load approaches zero in the circuit in Fig. 4, the volt-second product of L_{MX} also increases so that the circuit in Fig. 4 exhibits the maximum magnetizing current at no load, which makes it possible to achieve ZVS at no load.

Because magnetizing current i_{MX} does not contribute to the load current but flows between the two bridge legs, it represents a circulating current as seen in Fig. 4. Generally, this circulating current and its associated energy should be minimized to reduce losses and maximize conversion efficiency. Due to an inverse dependence of the volt-second product of L_{MX} on the load current, the circuit in Fig. 4 circulates less energy at full load than at light load, and, therefore, features ZVS in a wide load range with minimal circulating current.

To further understand the operation of the circuit in Fig. 4, Fig. 5 shows its key voltage and current waveforms when the circuit is implemented as a dc-dc converter. The waveforms in Fig. 5 are obtained based on analysis which assumes that output circuit Y comprises a low-pass LC filter, which has a large filter inductance L_F so that during a switching cycle the reflected load current into the primary of transformer T_Y is constant, as shown in Fig. 5. As can be seen from waveforms in Fig. 5, for all four primary switches S_1 through S_4 the magnitude of the current flowing through the switch at the turn-off moment is the same, i.e.,

$$|i_1(T_1)| = |i_2(T_4)| = |i_1(T_7)| = |i_2(T_{10})| = \left| \frac{i_{PY}}{2} \right| + |I_{MX}| \quad (9)$$

where I_{MX} is the amplitude of the magnetizing current i_{MX} .

According to (9), commutation of the switches in both legs is done by the energy stored by primary current i_{PY} and magnetizing current i_{MX} during the period when the capacitance of the turned-off switch is charging (voltage across the switch is increasing) and the capacitance of the switch that is about to be turned on is discharging (voltage across the switch is decreasing). While the commutation energy contributed by magnetizing current i_{MX} is always stored in magnetizing inductance L_{MX} of transformer T_X , the commutation energy contributed by current i_{PY} is stored either in the filter inductance of output circuit Y, or leakage inductances of transformers T_X and T_Y . Specifically, for leading-leg switches S_1 and S_2 , the commutation energy contributed by i_{PY} is stored in output-filter inductor L_F , whereas for lagging-leg switches S_3 and S_4 it is stored in the leakage inductance of the transformers. Since it is desirable to minimize the leakage inductance of transformer T_Y to minimize the secondary-side parasitic ringing, the energy stored in its leakage inductances is relatively small, i.e., much smaller than the energy stored in the output-filter inductance. As a result, in the circuit in Fig. 4, it is easy to achieve ZVS of leading-leg switches S_1 and S_2 in the entire load range, whereas ZVS of lagging-leg switches S_3 and S_4 requires a proper sizing of magnetizing inductance L_{MX} since at light loads almost entire energy required to create the ZVS condition of lagging-leg switches S_3 and S_4 is stored in the magnetizing inductance.

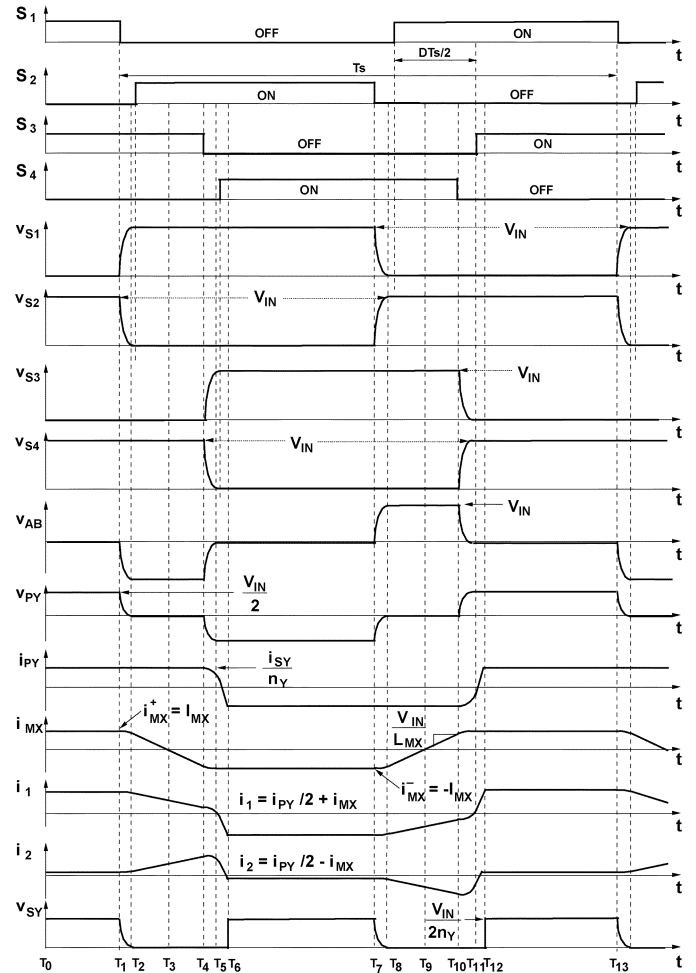


Fig. 5. Key waveforms of circuit in Fig. 4.

A similar analysis can be performed by assuming that output X of the circuit in Fig. 2 is regulated. A simplified circuit diagram when output X is regulated is shown in Fig. 6. In the simplified circuit in Fig. 6, it is assumed that only energy stored in the magnetizing inductance of transformer T_Y of the unregulated output is used to create the ZVS condition. Since no energy stored in the filter-inductor of output circuit Y is used to create the ZVS condition, output circuit Y is not shown in Fig. 6, which represents the preferred implementation due to a minimum component count. Furthermore, because of the absence of output circuit Y, transformer T_Y operates with the secondary winding opened, i.e., only the primary winding of the transformer is involved in the operation of the circuit. Therefore, in the circuit in Fig. 6, transformer T_Y operates as an inductor. In the simplified circuit in Fig. 6, this inductor is modeled by inductance L_{MY} . Also, in Fig. 6, the magnetizing inductance of transformer T_X is neglected because it has no important role in the operation of the circuit.

With reference to Fig. 6, the following relationships between currents can be established:

$$N_{PX}i_1 - N_{PX}i_2 - N_{SX}i_{SX} = 0, \quad (10)$$

$$i_{MY} = i_1 + i_2. \quad (11)$$

Solving (10) and (11) for i_1 and i_2 gives

$$i_1 = \frac{i_{MY}}{2} + \frac{i_{SX}}{2n_X}, \quad (12)$$

$$i_2 = \frac{i_{MY}}{2} - \frac{i_{SX}}{2n_X} \quad (13)$$

where $n_X = N_{PX}/N_{SX}$ is the turns ratio of transformer T_X .

As can be seen from (12) and (13), as in the case of implementation in Fig. 4, currents of both bridge legs i_1 and i_2 are composed of two components: load-current component $i_{SX}/2n_X$ and magnetizing-current component $i_{MY}/2$. The load-current component is directly dependent on the load current, whereas the magnetizing current does not directly depend on the load but rather on the volt-second product across the magnetizing inductance. Since in the circuit in Fig. 6 the phase shift decreases as the load approaches zero, the volt-second product of L_{MY} also increases so the circuit in Fig. 6 exhibits the maximum magnetizing current at no load, which makes it possible to achieve ZVS at no load.

As can be seen from Fig. 6, magnetizing current i_{MY} does not contribute to the load current because half of this current flows through primary windings AC and CB of transformer X in opposite directions. Therefore, current i_{MY} represents a circulating current that should be minimized. Due to an inverse dependence of the volt-second product of L_{MY} on the load current, the circuit in Fig. 6, likewise the circuit in Fig. 4, circulates less energy at full load than at light load and, therefore, features ZVS in a wide load range with a minimum circulating current.

Fig. 7 shows key current and voltage waveforms of the circuit in Fig. 6, when the circuit is implemented as a dc–dc converter. The waveforms in Fig. 7 are obtained by assuming that output circuit X comprises a low-pass LC filter, which has a large filter inductance L_F so that during a switching cycle the reflected load current into the primary of transformer T_X is constant, as shown in the waveform in Fig. 7. As can be seen from waveforms in Fig. 7, for all four primary switches S_1 through S_4 the magnitude of the current flowing through the switch at the turn-off moment is the same, i.e.,

$$|i_2(T_1)| = |i_1(T_4)| = |i_2(T_7)| = |i_1(T_{10})| = \left| \frac{i_{SX}}{2n_X} \right| + \left| \frac{I_{MY}}{2} \right| \quad (14)$$

where I_{MY} is the amplitude of the magnetizing current i_{MY} .

However, it should be noted that opposite from the implementation in Fig. 4, in the implementation in Fig. 6 the energy for creating the ZVS condition of lagging-leg switches S_3 and S_4 is stored in the output filter inductor, whereas the energy for creating the ZVS condition of leading-leg switches S_1 and S_2 is stored in the leakage inductances of transformer T_X and in the inductance L_{MY} . Therefore, in the circuit in Fig. 6, it is harder to achieve ZVS of the leading-leg switches than the lagging-leg switches. In fact, since almost all energy for zero-voltage commutation of leading-leg switches S_1 and S_2 is stored in inductance L_{MY} , to achieve ZVS of the leading-leg switches in a wide load range, a proper sizing of the magnetizing inductance L_{MY} is required.

From the generalized circuit in Fig. 2, a family of FB ZVS-PWM circuits can be derived. Figs. 8–10 shows some

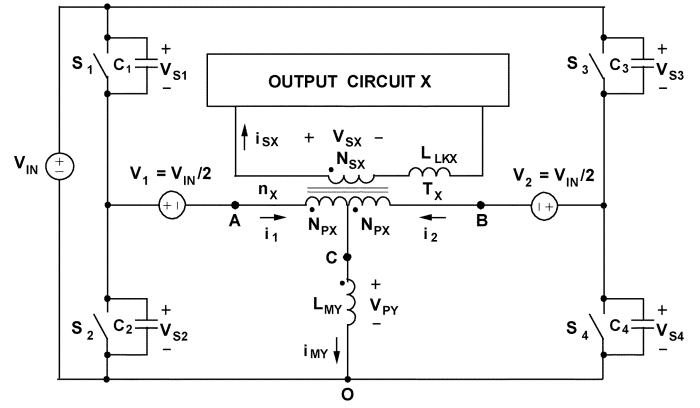


Fig. 6. Simplified circuit diagram of converter in Fig. 2 when output X is regulated.

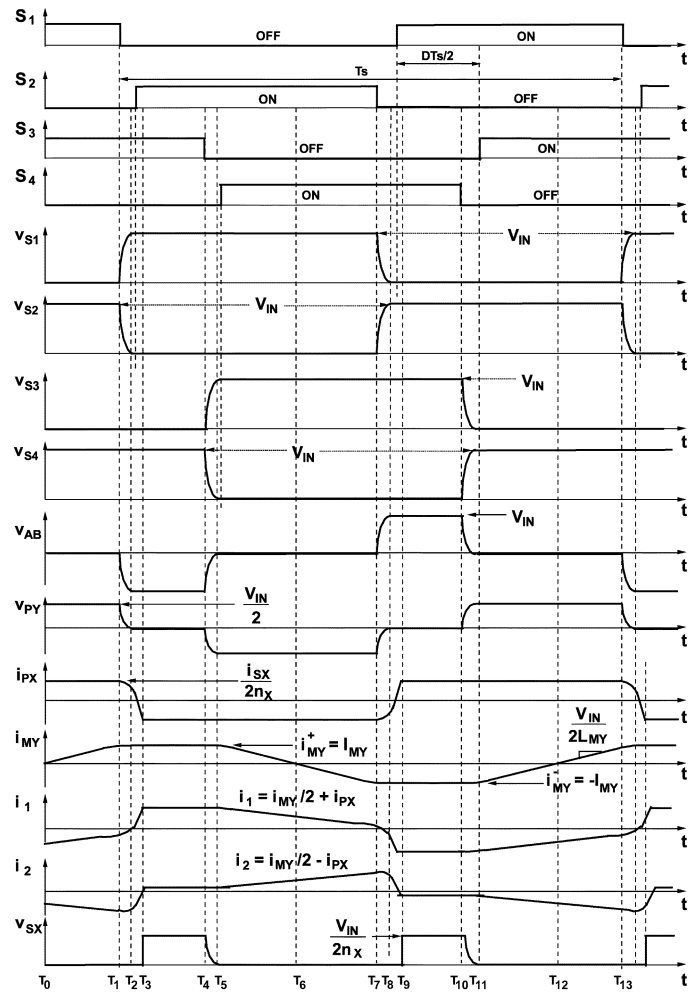


Fig. 7. Key waveforms of circuit in Fig. 6.

examples of these circuits implemented as dc–dc converters. The circuit in Fig. 8 is derived from the circuit in Fig. 4 by implementing output circuit Y with a full-wave rectifier. Transformer T_X of the unregulated output is implemented as coupled inductor L_C , whereas voltage sources V_1 and V_2 are implemented with capacitors C_{B1} and C_{B2} , respectively. Namely, if capacitors C_{B1} and C_{B2} are large enough so that the resonant frequency of the series resonant circuit formed by

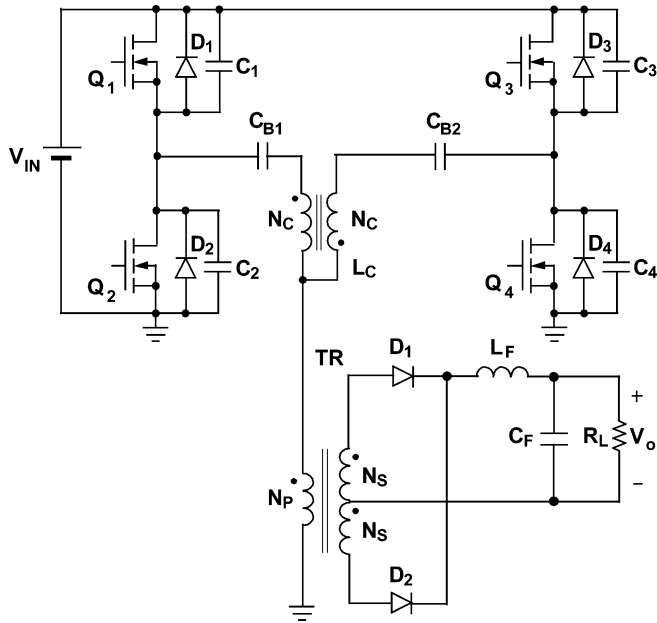


Fig. 8. Implementation of FB ZVS-PWM converter derived from circuit in Fig. 4 when Y is regulated output.

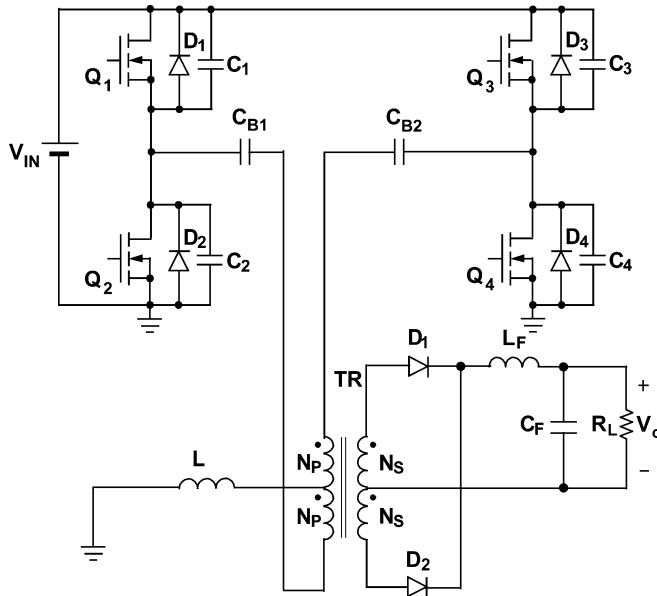


Fig. 9. Implementation of FB ZVS-PWM converter derived from circuit in Fig. 6 when X is regulated output.

these capacitors and the magnetizing inductance of L_C is much smaller than the switching frequency, then the voltage across capacitors is constant and equal to $V_{IN}/2$. It also should be noted that the circuit in Fig. 8 can also be implemented with other types of the secondary-side rectifier circuit, such as the current-doubler rectifier.

Fig. 9 shows the implementation of the FB ZVS-PWM converter according to the circuit in Fig. 6 when X is regulated output. This converter employs capacitors C_{B1} and C_{B2} to implement source V_1 and V_2 . It should be noted that the circuits in Fig. 8 uses coupled inductor L_C to store energy for ZVS, whereas inductor L in the circuit in Fig. 9 is uncoupled.

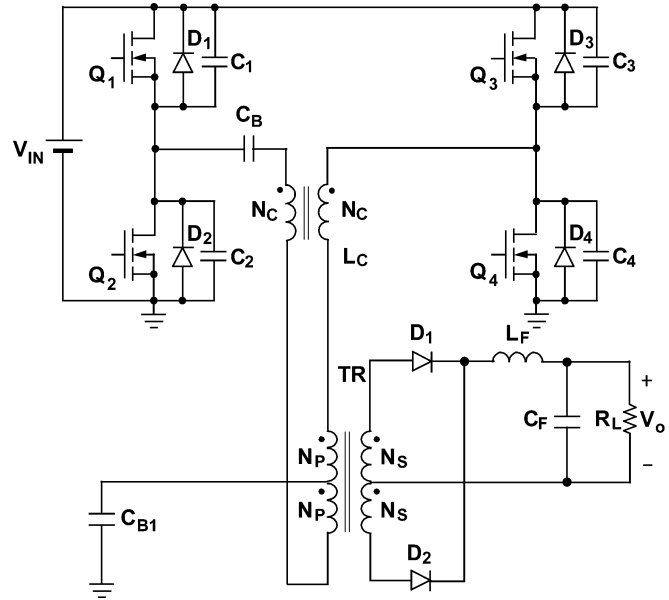


Fig. 10. Another implementation of FB ZVS-PWM converter derived from circuit in Fig. 6 when X is regulated output.

Fig. 10 shows another topology derived from the circuit in Fig. 6. In this topology, voltage sources V_1 and V_2 are shifted from the respective primaries of transformer T_X into the primary of transformer T_Y . Since this circuit transformation does not change any of the circuit's branch currents and node voltages, it also does not change the waveforms of the circuit. As a result, voltage sources V_1 and V_2 are implemented with single capacitor C_{B1} in Fig. 10. However, to prevent the saturation of transformer T_X , which happens when the switching waveforms of the bridge legs are not identical, capacitor C_B is connected in series with transformer T_X , i.e., coupled inductor L_C . Generally, the voltage across capacitor C_B is small (close to zero) since this capacitor only takes on the voltage difference caused by a mismatching of the bridge legs, which is usually small.

III. DESIGN GUIDELINES

To achieve ZVS of the converter shown in Fig. 2, the sum of the energy stored in the leakage inductance of the transformer in the regulated output and the magnetizing inductance of the transformer in the unregulated output must be more than or equal to the energy required to discharge the capacitances of the switches which are about to be turned on and off. At heavier load currents, ZVS is primarily achieved by the energy stored in the residual leakage inductances of the transformers in the regulated output. As the load current decreases, the energy stored in the leakage inductances also decreases, whereas the energy stored in the magnetizing inductance of the transformer of the unregulated output increases so that at light loads this magnetizing inductance provides an increasing share of the energy required for ZVS. In fact, at no load, the magnetizing inductance provides the entire energy required to create the ZVS condition. Therefore, if the value of the magnetizing inductance of the transformer in the unregulated output is selected so that ZVS is achieved at no load and maximum input voltage $V_{IN(max)}$, ZVS is achieved in the entire load and input-voltage range.

Neglecting the capacitances of the transformer’s windings, the value of magnetizing inductance L_{MY} required to achieve ZVS of leading-leg switches in the implementations where output X is regulated is calculated in [12, p. 237] as

$$L_{MY} \leq \frac{1}{128Cf_S^2} \quad (15)$$

whereas, the value of magnetizing inductance L_{MX} necessary to achieve ZVS of lagging-leg switches in the implementations where output Y is regulated can be calculated following the same calculation procedure as

$$L_{MX} \leq \frac{1}{32Cf_S^2} \quad (16)$$

where C is the total capacitance across the primary switches (parasitic and external capacitance, if any) in the corresponding legs.

The control of the proposed circuits is the same as that of the conventional constant-frequency FB ZVS-PWM converter. In fact, any of the integrated phase-shift controllers available on the market can be used to implement the control of the proposed circuit. However, it should be noted that in the circuits with regulated output Y, the maximum output voltage (volt-second product) is obtained when the bridge legs are operated in phase (0° phase shift), whereas the maximum output voltage (volt-second product) for the circuits with regulated output X occurs when the bridge legs are operated in antiphase (180° phase shift). This difference in the control characteristics of the two circuit implementations has a minor effect on the control loop design since a simple control-signal inversion in the voltage control loop solves the problem.

IV. EXPERIMENTAL RESULTS

The performance of the proposed circuit shown in Fig. 8 was verified on a 670-W experimental prototype operating at 112 kHz, as reported in [12]. The experimental converter was designed to operate from 400-V dc input and deliver 14 A from a 48-V output. The phase-shift control circuit was implemented using a UC3875 controller. Fig. 11 shows the measured waveforms of the proposed FB ZVS converter. As can be seen from the waveforms in Fig. 11, the proposed converter has a very small duty cycle loss ($<4\%$), as well as a small parasitic ringing because of a minimized leakage inductance of the transformer that is less than $2 \mu\text{H}$ on the primary side.

The proposed converter shows a conversion efficiency improvement in the entire measured power range as shown in Fig. 12. Generally, the efficiency improvement is more pronounced at light loads where the conventional FB ZVS converter operates with hard switching. The measured efficiency is approximately 89% at 10% load and 95% at full load.

V. CONCLUSION

A new family of isolated, constant-frequency, phase-shift FB ZVS-PWM converters that can achieve complete ZVS in a wide range of load current and input voltage is introduced. The introduced FB ZVS-PWM family employs an auxiliary circuit in which the energy that is used for creating the ZVS condition is

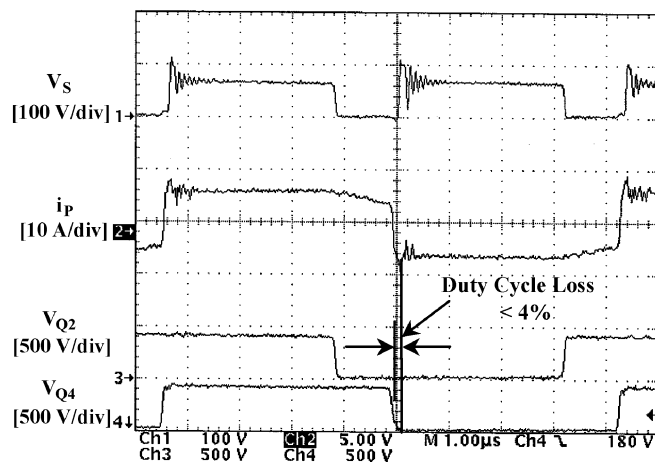


Fig. 11. Measured key waveforms at $P_O = 670 \text{ W}$. From top to bottom: secondary voltage V_S ; primary current i_P ; drain-to-source voltage V_{Q2} of Q_2 ; drain-to-source voltage V_{Q4} of Q_4 . Time base: $1 \mu\text{s}/\text{div}$.

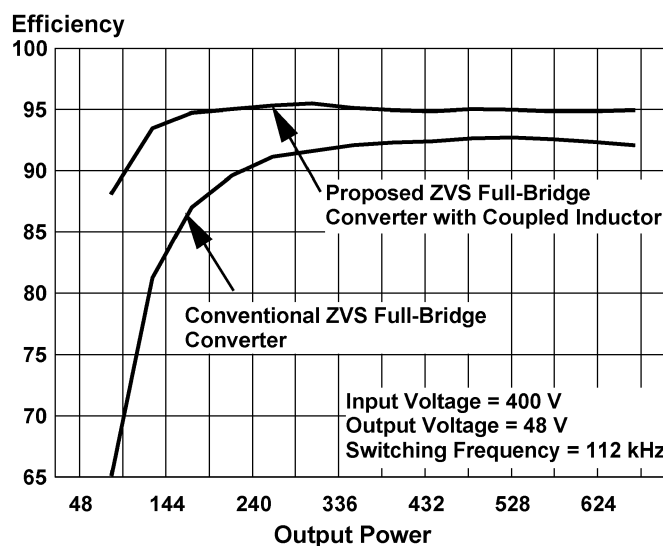


Fig. 12. Measured efficiencies of conventional FB ZVS converter and proposed FB ZVS converter as functions of output power [12].

not only dependent on the input voltage, but is also dependent on the load. Specifically, the auxiliary circuit provides very little energy at full load, whereas it provides maximum energy for ZVS at no-load. In the auxiliary circuit in the proposed family of FB ZVS-PWM converters, the energy-storage component is an inductor that is either coupled or uncoupled. Since this inductor does not appear in the power-transfer path, i.e., does not carry the load current, it also does not cause a loss of duty cycle or voltage ringing across the output rectifiers.

REFERENCES

- [1] O. D. Patterson and D. M. Divan, "Pseudo-resonant full bridge dc/dc converter," in *Proc. IEEE PESC'87 Conference*, 1987, pp. 424–430.
- [2] R. A. Fisher, K. D. T. Ngo, and M. H. Kuo, "A 500 kHz, 250 W dc-dc converter with multiple outputs controlled by phase-shifted PWM and magnetic amplifiers," in *Proc. High Frequency Power Conversion Conference*, May 1988, pp. 100–110.
- [3] L. H. Mweene, C. A. Wright, and M. F. Schlecht, "A 1 kW, 500 kHz front-end converter for a distributed power supply system," in *Proc. IEEE APEC'89 Conference*, 1989, pp. 423–432.

- [4] D. B. Dalal, "A 500 kHz multi-output converter with zero voltage switching," in *Proc. IEEE APEC'90 Conference*, 1990, pp. 265–274.
- [5] R. Redl, N. O. Sokal, and L. Balogh, "A novel soft-switching full-bridge dc/dc converter: analysis, design considerations, and experimental results at 1.5 kW, 100 kHz," in *Proc. IEEE PESC'90 Conference*, 1990, pp. 162–172.
- [6] J. A. Sabaté, V. Vlatković, R. B. Ridley, and F. C. Lee, "High-voltage, high-power, ZVS, full-bridge PWM converter employing an active snubber," in *Proc. IEEE APEC'91 Conference*, 1991, pp. 158–163.
- [7] W. Chen, F. C. Lee, M. M. Jovanović, and J. A. Sabaté, "A comparative study of a class of full bridge zero-voltage-switched PWM converters," in *Proc. IEEE APEC'95 Conference*, 1995, pp. 893–899.
- [8] M. Nakaoka, S. Nagai, Y. J. Kim, Y. Ogino, and Y. Murakami, "The state-of-the art phase-shifted ZVS-PWM series & parallel resonant dc-dc power converters using internal parasitic circuit components and new digital control," in *Proc. IEEE PESC'92 Conference*, 1992, pp. 62–70.
- [9] P. K. Jain, W. Kang, H. Soin, and Y. Xi, "Analysis and design considerations of a load and line independent zero voltage switching full bridge dc/dc converter topology," *IEEE Trans. Power Electron.*, vol. 17, pp. 649–657, Sept. 2002.
- [10] J. G. Cho, J. A. Sabaté, and F. C. Lee, "Novel full bridge zero-voltage-transition PWM dc/dc converter for high power application," in *Proc. IEEE APEC'94 Conference*, 1994, pp. 143–149.
- [11] R. Ayyanar and N. Mohan, "Novel soft-switching dc-dc converter with full ZVS-range and reduced filter requirement—part I: regulated-output applications," *IEEE Trans. Power Electron.*, vol. 16, pp. 184–192, Mar. 2001.
- [12] Y. Jang and M. M. Jovanović, "A new ZVS-PWM full-bridge converter," in *Proc. IEEE International Telecommunications Energy Conf. (INT-ELEC'02)*, 2002, pp. 232–239.



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