Single-Stage Flyback LED Driver Meets Class C Limits on Harmonic Currents

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The technology and performance of high-brightness light-emitting diodes (HB LEDs) have undergone significant improvements driven by new applications in liquid-crystal-display (LCD) backlighting, automotive lighting, traffic lights, and general-purpose lighting [1]-[3]. As a solid-state light source that does not contain mercury, HB LEDs have been widely accepted because of their superior longevity, low-maintenance requirements, and continuously-improving luminance with a great potential to replace existing lighting sources such as incandescent and fluorescent lamps in the future.

For input-power levels above 25 W, ac-dc LED drivers must comply with the line-current harmonic limits set by the IEC 61000-3-2 Class C [4] and the corresponding Japanese JIS C 61000-3-2 Class C [5] regulations. Generally, it is difficult to meet these requirements by employing passive power-factor-correction (PFC) techniques, especially for applications with the universal input voltage range (90 to 270 Vrms). As a result, the majority of today's universal-input ac-dc LED drivers are implemented with active PFC.

A conventional two-stage LED driver with active PFC is shown in Fig. 1. The first stage provides a near unity power factor and a low total harmonic distortion (THD) across the entire universal input voltage range, while the second, dc-dc stage is used to provide a tight regulation of the output.

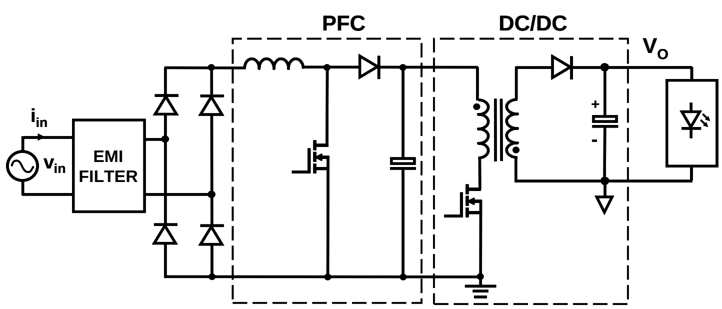

Fig. 1. Conventional two-stage LED driver.

Since the circuit in Fig. 1 requires two independently controlled power switches and two control circuits, it suffers from an increased component count and cost. In low-power lighting applications, where the cost is the dominant consideration, the two-stage approach is less competitive than single-stage active PFC implementations [6], [7], where the PFC stage is integrated with the dc-dc stage. Moreover, due to its minimal component count and low cost, the single-stage, single-switch, PFC flyback converter [8], [9] has emerged as the most widely used single-stage topology.

Generally, a single-stage PFC ac-dc converter can be implemented without or with a bulk capacitor at the primary side, as illustrated in Figs. 2 and 3, respectively. Although the single-stage PFC circuit in Fig. 2 [8] has the advantage of a lower component count, its output voltage has a high ripple at twice the line frequency unless very large output capacitors are used. For an LED load, a small variation in the driving voltage can lead to a large variation in the LED current, and a large ripple of the LED current would seriously affect the reliability and longevity [10], as well as the luminous efficacy [11] of the LEDs. Therefore, the approach in Fig. 2 often requires a post-regulator, which adds cost and lowers the efficiency.

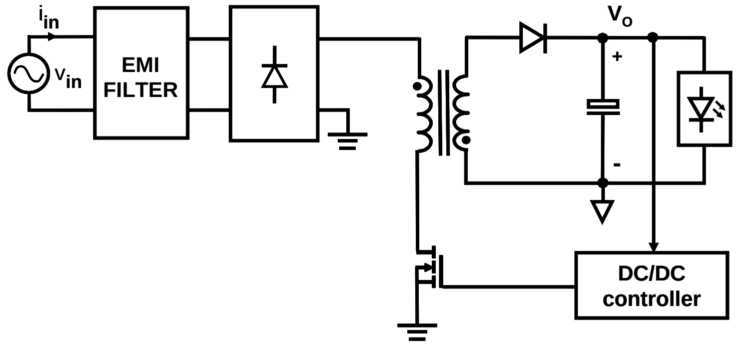

Fig. 2. Single-stage flyback LED driver without energy-storage capacitor at primary side.

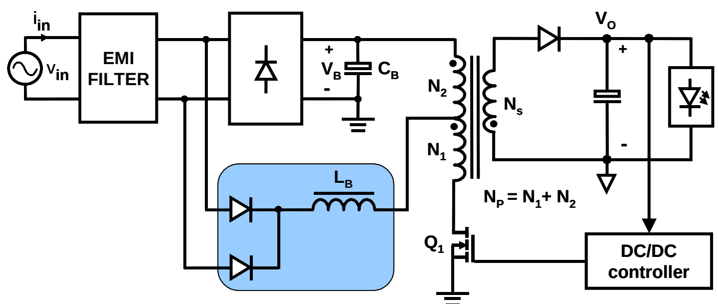

Fig. 3. Single-stage flyback LED driver with energy-storage capacitor at primary side.

The single-stage PFC flyback topology shown in Fig. 3 [9] presents one of the most cost-effective single-stage solutions. In this converter, a PFC boost stage is integrated with the dc-dc flyback stage. The PFC boost stage operates in discontinuous conduction mode (DCM), while the dc-dc flyback stage operates at the DCM/CCM (continuous-conduction-mode) boundary. A low input-current harmonic distortion can be achieved due to the inherent property of the DCM PFC boost converter to draw a near sinusoidal current if its duty cycle is held relatively constant during a half line cycle. However, voltage V_B across bulk capacitor C_B is not regulated and at high line it can increase to impractical levels.

To reduce the bulk capacitor voltage, one terminal of the boost inductor winding is connected to a tapping point of the primary winding of the flyback transformer, which provides a negative magnetic feedback [12]. However, the tapping of the flyback primary winding also results in a zero-crossing distortion of the line current. In fact, as long as the instantaneous line voltage is lower than the voltage at the tapping point, no current is drawn from the input, which reduces the power factor and increases the line-current harmonics. Therefore, the selection of the tapping point is determined by the tradeoff between the reduction of the bulk-capacitor voltage and the quality of the line current.

The single-stage PFC flyback in Fig. 3 has been successfully applied in adapter and charger applications for the universal line voltage, where the line-current harmonics only need to meet the IEC 61000-3-2 and JIS C 61000-3-2 Class D limits, which are less stringent than the corresponding Class C limits.

It was shown in [13] and [14] that the single-stage PFC flyback in Fig. 3 with a constant boost inductance cannot be designed to achieve a practical maximum bulk-capacitor voltage level (i.e., less than 450 V) at high line while meeting the JIS C 61000-3-2 Class C line-current harmonic limits at low line. To overcome these limitations, a variable boost inductance is required, i.e., a high boost inductance at high line to limit the bulk-capacitor voltage and a lower boost inductance at low line to ensure DCM operation and, consequently, a low THD.

In fact, at low line, when a constant boost inductance is used, the inductor will enter CCM operation around the peak of the line voltage, and the line-current waveform will have a surge around its peak value [13], resulting in an increased THD. Furthermore, if the bulk-capacitor voltage is slightly lower than the peak value of the rectified line voltage, the peak charging of the bulk capacitor through the bridge rectifier will also result in a surge in the line current waveform [12] with an increased THD.

The work in [14] shows that by optimizing the tapping point of the primary winding of the flyback transformer in Fig. 3 and by reducing the PFC boost inductance at low line, a high power factor and a low THD with relatively high efficiency can be achieved such that the line current harmonics satisfy the IEC 61000-3-2 and corresponding Japanese JIS C 61000-3-2 Class C limits, while the bulk capacitor voltage is limited below 400 V. The PFC boost inductance at low line was reduced through adding a bias magnetic field to the PFC inductor core using the load current. However, using the load current as the bias current leads to practical issues such as isolation between the primary and secondary sides, and difficulty in layout and assembly.

Other methods for achieving a variable inductor were introduced in [15] through [21]. The merits and demerits of those methods were detailed in [14] and [22]. This paper presents a practical primary-side-based bias-current and control circuit for the variable PFC boost inductor in a single-stage LED driver employing the same boost-inductor structure as in [14]. This approach allows the use of a bias-control switch with a lower cost since it does not need to have ultra-low turn-on resistance. The single-stage LED driver with the proposed variable boost inductor is experimentally verified on a 24-V, 91-W prototype circuit.

Single-Stage PFC Flyback LED Driver With Variable Boost Inductor

Fig. 4 shows the detailed schematic of the single-stage PFC flyback LED driver with the proposed variable boost inductor. The basic PFC boost inductor is implemented with an EE core and winding N_{LB}. A half core (E) with winding N_C is closely attached to the bottom part of the EE core. The boost inductance L_B is controlled by a bias current I_C, which is obtained via an auxiliary power supply consisting of winding N_4 of the flyback transformer, diode D_C and capacitor C_C.

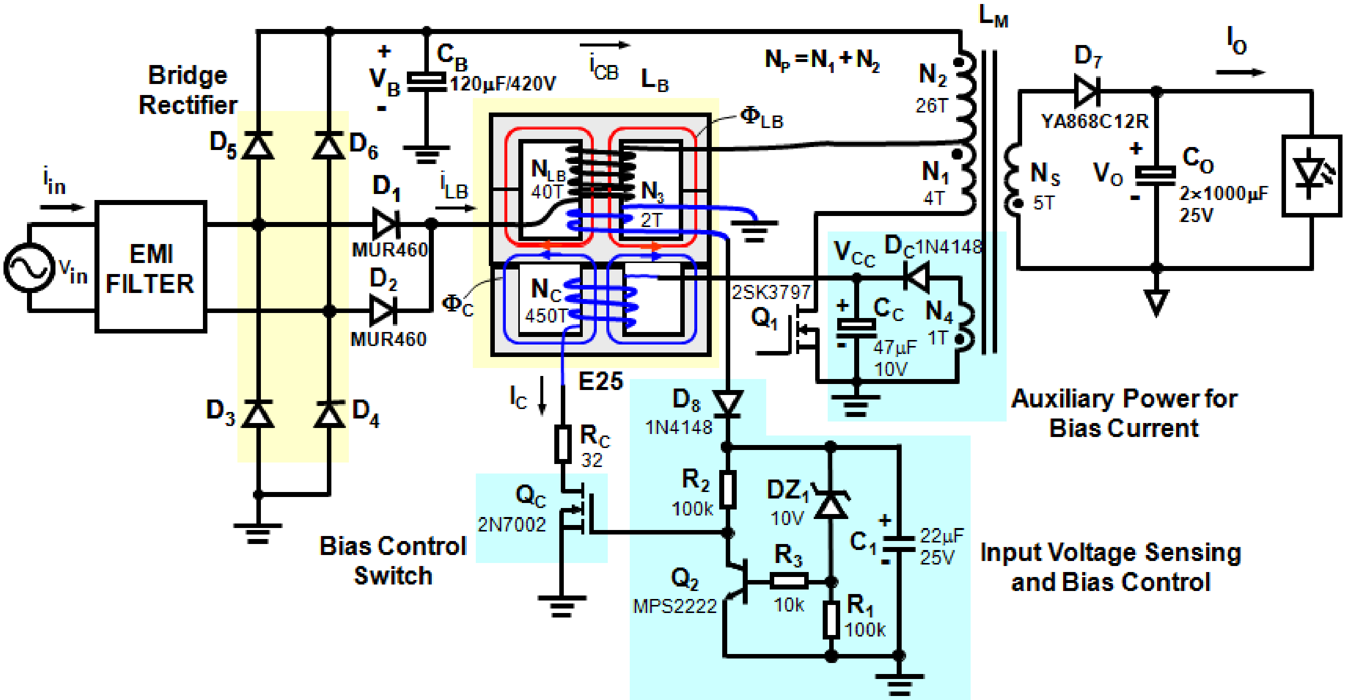

Fig. 4. Schematic of single-stage PFC flyback LED driver with proposed variable boost inductor.

The flow of current I_C is controlled by a switch Q_C, which is turned on and off by an input-voltage-sensing and bias-control circuit. At low line, switch Q_C is closed, and the bias current flows through bias winding N_C, inducing a magnetic flux Φ_C that is added to the main magnetic flux Φ_{LB} at the bottom part of the boost-inductor EE core. As a result, at the bottom part of the EE core, the effective permeability is reduced, and consequently, the boost inductance is decreased [14]. The reduction of the boost inductance is proportional to the applied bias current I_C, which is determined as

$$I_C = \frac{V_{C_C}}{R_C + R_{N_C} + R_{Q_C}} \qquad (1)$$

where $V_{Cc} = (N_4/N_S) \cdot V_O$ is the output voltage of the auxiliary power supply, R_C is the resistance in series with the bias winding N_C to adjust the bias current, R_{Nc} is the resistance of the bias winding N_C, and R_{Qc} is the on-resistance of bias control switch Q_C. At high line, switch Q_C is open, there is no bias current flowing through winding N_C, and the boost inductance does not change.

The input voltage is sensed by the circuit consisting of winding N_3 wound on the boost-inductor EE core, diode D_8, and capacitor C_1. When main switch Q_1 is turned on, diode D_8 is forward biased, peak charging capacitor C_1 with a voltage,

$$V_{C1} = (\sqrt{2}V_{IN} - \frac{N_1}{N_P}V_B)\frac{N_3}{N_{LB}} - V_{D8} \tag{2}$$

where N_1, N_P and N_{LB} are the numbers of turns of the feedback winding, primary winding of the flyback transformer, and the boost-inductor winding, respectively. A proper turns number N_3 ($N_3 = 2$) is chosen so that the voltage across capacitor C_1 turns on Zener diode DZ_1 ($V_{DZ1} = 10$ V) only at high line (180 to 270 Vrms). When DZ_1 is turned on, switch Q_2 is turned on and the gate-to-source voltage of switch Q_C is low, turning off Q_C. As a result, no bias current flows through control winding N_C and boost inductance does not change. At low line, voltage V_{C1} is lower than the turn-on voltage of DZ_1, Q_2 is turned off and the gate-to-source voltage of switch Q_C is high, turning on switch Q_C. As a result, bias current I_C flows through the control winding N_C and boost inductance decreases. Selection of respective PFC boost inductance at high line and low line follows the same procedure as described in [14].

Experimental Results

To verify the proposed variable boost-inductance technique, a 24-V, 91-W single-stage PFC flyback prototype for LED applications was built. The control circuit is based on the quasi-resonant controller NCP1207 from ON Semiconductor. Parameters of key components are: L_M = 645 µH, L_B = 400 µH, N_1 = 4 turns, N_2 = 26 turns, N_3 = 1 turn, N_S = 5 turns, N_C = 450 turns (AWG#32, R_{NC} = 13.8 Ω), R_C = 32 Ω, Q_1: 2SK3797 (600 V, 13 A), Q_C: 2N7002 (60 V, 0.5 A). At V_O = 24 V, the dc bias voltage is 4.8 V, resulting in a power loss of 0.43 W at low line caused by the total series-resistance ($R_C + R_{Nc} + R_{Qc}$ = 53.3 Ω) of the bias circuit. The measured line-voltage and line-current waveforms at full load (24 V, 3.8 A) are shown in Fig. 5.

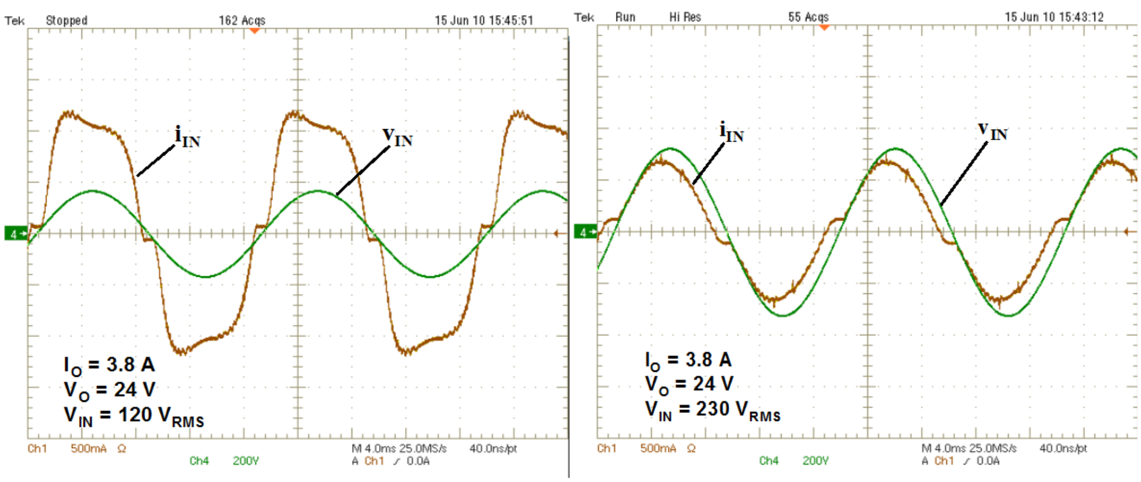

Fig. 5. Measured line-current (500 mA/div) and line-voltage (200 V/div) waveforms at V_{IN} = 120 Vrms and V_{IN} = 230 Vrms.

The measured line-voltage and line-current waveforms at full load (24 V, 3.8 A) are shown in Fig. 5. At nominal low line (120 Vrms), THD = 15%, PF = 0.98, V_B = 183 V, and efficiency = 88%; while at nominal high line (230 Vrms), THD = 11%, PF = 0.97, V_B = 327 V, and efficiency = 91% were obtained. Measurements at both full load and light load (P_{IN} = 25 W) show that the line-current harmonics satisfy the IEC 61000-3-2 and JIS C 61000-3-2 Class C limits with enough margin. Fig. 6 shows the measured line current harmonics at full load. The measured efficiency versus output power is shown in Fig. 7. It should be noted that the measured efficiency at full load is well above 85%, which is the typical requirement at full load.

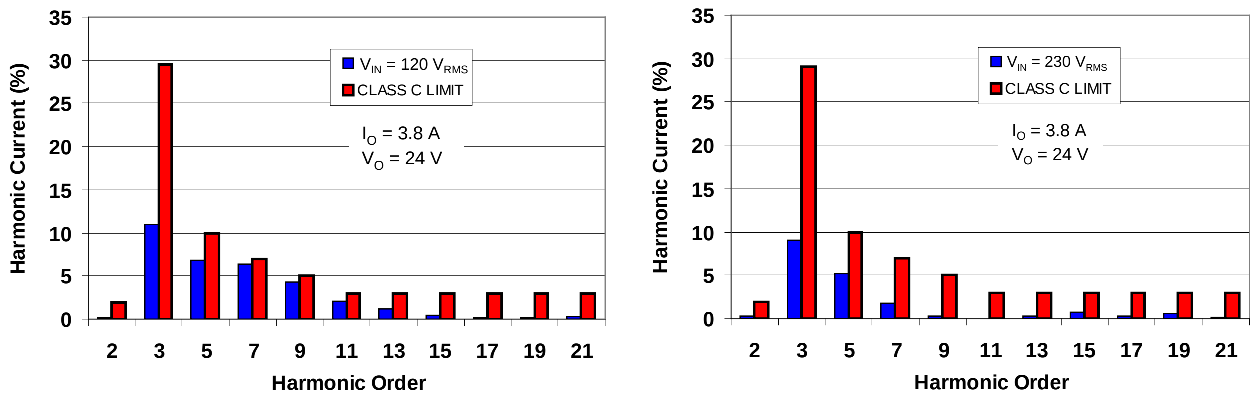

Fig. 6. Measured line-current harmonics at V_{IN} = 120 Vrms and V_{IN} = 230 Vrms.

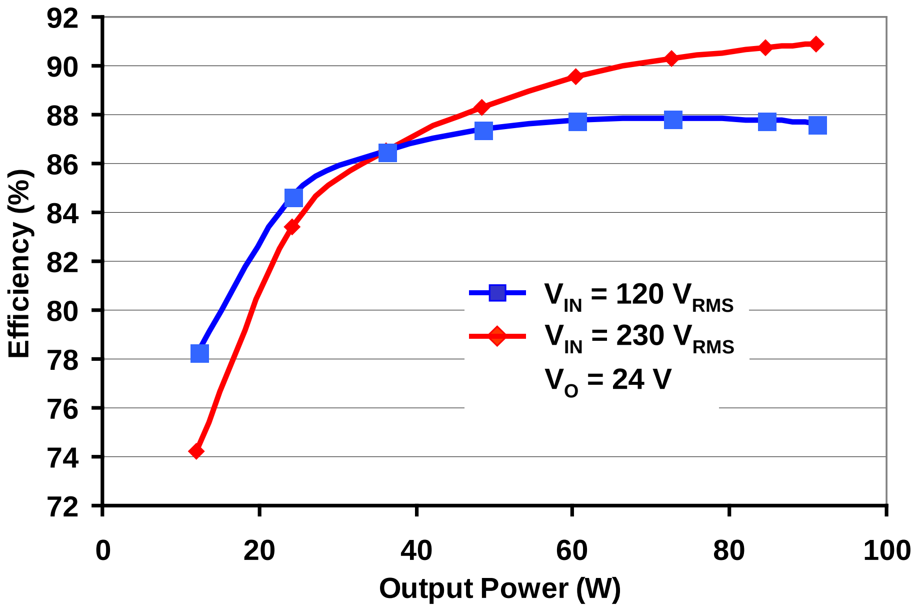

Fig. 7. Measured efficiency vs. output power.

Measurements with an actual LED load were also performed. Four LED strings each with seven series-connected white LEDs (Philips Lumileds, LXHL-LW3C) were paralleled and directly driven by the proposed PFC flyback prototype with an output voltage of 24 V. The measured LED-current waveform at nominal low line (120 Vrms) is shown in Fig. 8. The peak-to-peak value of the ac ripple current is 3.8% of the full load current (3.8 A). At nominal high line (230 Vrms), the measured peak-to-peak ac ripple current is 2.7% of the full load current. Measured maximum bulk-capacitor voltage V_B at V_{IN} = 270 Vrms is 403 V.

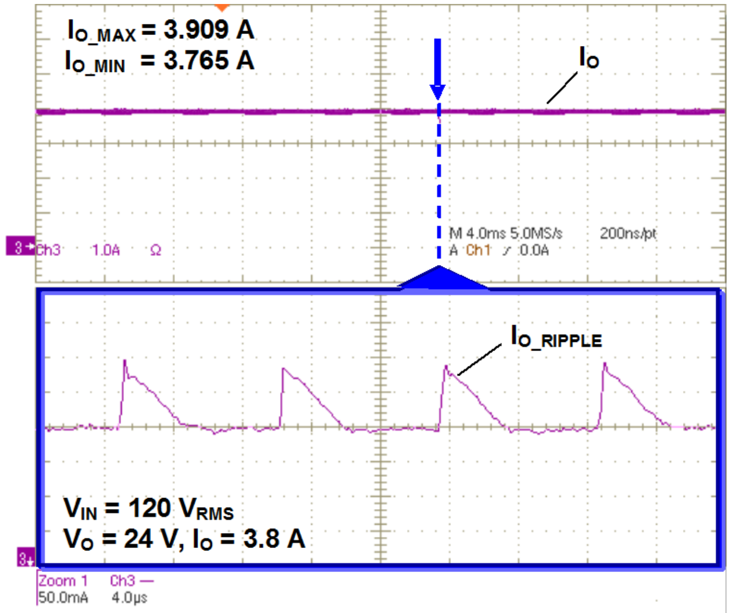

Fig. 8. Measured waveform of LED current at nominal low line (120 Vrms) and full load. Top trace: I_O [1 A/div, 4 ms/div]; Bottom trace: I_{O_RIPPLE} [50 mA/div, 4 µs/div].

Summary

A single-stage PFC flyback LED driver with a variable PFC boost inductance for the universal input voltage is presented in this paper. The PFC boost inductance has a constant high value at high line, while at low line it is reduced to a lower value, which is achieved by adding a bias magnetic field (generated by a primary-side bias current) in the magnetic core of the PFC boost inductor.

Experimental results obtained on a 24-V, 91-W prototype show that the proposed LED driver achieves an efficiency of 88%, a power factor of 0.98 and a THD of 15% at nominal low line (120 Vrms), and an efficiency of 91%, a power factor of 0.97 and a THD of 11% at nominal high line (230 Vrms). Line-current harmonics satisfy the IEC 61000-3-2 and corresponding Japanese JIS C 61000-3-2 Class C limits with enough margin at both full load and light load (P_{IN} = 25 W). Therefore, the proposed single-stage PFC flyback circuit is suitable for directly driving LED strings, yet requires no post-regulators. This capability is a significant advantage over the conventional PFC flyback circuit without an energy-storage capacitor on the primary side.

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