Hold-Up Time Extension Circuit With Integrated Magnetics

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Abstract—A circuit that substantially extends the hold-up time of ac–dc power supplies is introduced. By using integrated magnetics, the power density of this hold-up time extension circuit is maximized. The performance of the proposed approach was evaluated on a universal line range 1-kW power supply.

Index Terms—AC–DC power supply, boost converter, hold-up time, magnetic integration.

I. INTRODUCTION

As the required power and density of ac–dc computer power supplies increase, the size of the hold-up time energy-storage (bulk) capacitors, which store the energy that is used to deliver power to the load for a short time (typically 10–20 ms) after a line dropout, becomes a significant factor in limiting the maximum attainable power density. Therefore, the minimization of the hold-up-time capacitor size is an indispensable design step in maximizing the power density of ac–dc computer power supplies. The minimization of the size of the hold-up-time capacitors can be accomplished by advancements in capacitor technology that would increase the volumetric efficiency ($\mu F/in^3$) of the energy-storage capacitors and/or by circuit optimization techniques that would minimize the amount of capacitance needed for a given hold-up time.

So far, two techniques for minimization of the hold-up-time capacitor size without efficiency degradation are proposed and demonstrated [1]–[3]. The technique described in [1] employs variable transformer-turns-ratio concept, whereas in the technique introduced in [2] and reintroduced in [3] employs a hold-up-time extension circuit to maximize the utilization of the stored energy.

In the variable-turns-ratio approach the effective turns ratio of the transformer is controlled by a secondary-side switch [1]. When the ac line voltage is present, the secondary-side switch is off and the primary-to-secondary turns ratio of the transformer is maximal, which maximizes the conversion efficiency. During the hold-up-time mode, i.e., during the ac line dropout, the secondary-side switch is closed to effectively increase the number of turns of the secondary winding. As a result, the turns ratio of the transformer is reduced, which allows the converter to operate down to a lower bulk capacitor voltage so that the utilization of the energy stored in the bulk capacitors is optimized. The variable-turns-ratio approach is a very cost-effective approach since it requires a minimal number of additional components. A potential deficiency of this approach is the concern that the abrupt change of the turns ratio of the transformer at the moment the secondary-switch is turned on may cause out-of-spec deviations of the output-voltage, especially in low-output-voltage applications. In addition, this concept is not suitable for applications in multiple-output power supplies because it would require a separate switch and windings for each output.

In the hold-up-time extension circuit approach, the improved utilization of the stored bulk-capacitor energy is obtained by employing an additional dc–dc boost-type converter [2]. This hold-up-time extension converter that is connected at the input of the dc–dc output stage is only active during hold-up time period, i.e., when the ac line is absent and the front-end power-factor-correction (PFC) circuit does not deliver power. Otherwise, it is turned off and shorted out of the power-delivery path. To provide energy at the input of this hold-up time extension circuit the total bulk capacitance is split in two. The larger part of this capacitance is connected at the input of the hold-up-time extension circuit, whereas the smaller part is connected at the output of the hold-up-time extension circuit, i.e., the input of the dc–dc output stage.

Since the hold-up-time extension circuit is connected at the input of the dc–dc output stage, its performance and complexity is unaffected by the dc–dc output stage topology and number of outputs. In addition, since the hold-up-time extension circuit acts outside the control loop of the dc–dc output stage, the dc–dc output(s) are virtually immune to the disturbance that may be generated at the moment the hold-up-time extension circuit is activated. The major drawback of hold-up-time-extension approach is that its implementation requires additional power-stage and control-circuit components. In particular, it requires an additional energy-storage inductor for the implementation of the boost-type hold-up-time extension circuit, which has detrimental effect on attainable power density.

In this paper, an integrated magnetics approach that eliminates the need for a separate hold-up-time extension inductor is presented. The operation and performance of the proposed hold-up-time extension circuit with integrated magnetics was verified on a 1-kW prototype.

II. BULK ENERGY UTILIZATION ANALYSIS

Fig. 1(a) shows the block diagram of a conventional off-line power supply with energy storage capacitor $C_B$. The required energy to support the output during the hold-up time is obtained from a properly sized energy-storage capacitor $C_B$. Generally, the front-end rectifier can either be a simple full-wave diode rectifier or a rectifier with an active PFC circuit.
To achieve the desired hold-up time, the dc–dc converter output stage in Fig. 1(a) must be designed to operate until energy storage capacitor voltage \( V_B \) reaches a voltage that is lower than minimum energy-storage capacitor voltage \( V_{BMIN} \). With such a design for the dc–dc output stage, the energy storage capacitor will deliver power to the output after a line dropout until the energy-storage capacitor discharges to \( V_{BMIN} \), as illustrated in Fig. 1(b). The relationship between the value of energy-storage capacitor \( C_B \) and hold-up time \( T_H \) is given by

\[
C_B = \frac{2 \cdot P_{OH}}{V_{BH}^2 - V_{BMIN}^2} \cdot \frac{T_H}{V_{BH}}
\]  

where \( P_{OH} \) is the amount of output power that needs to be provided during hold-up time \( T_H \) and \( V_{DC-DC} \) is the efficiency of the dc–dc converter output stage.

As can be seen from (1), for a given \( V_{BH} \) and \( V_{BMIN} \), the larger the power \( P_{OH} \) and/or the longer the hold-up time \( T_H \), the larger the energy-storage capacitor \( C_B \) needs to be used. As a result, in high-power applications, the size of the energy-storage capacitor(s) often limits the maximum power density. Therefore, to maximize power density, the size of the energy-storage capacitors must be minimized. A size reduction of energy-storage capacitor \( C_B \), shown in Fig. 1, can be achieved by extending the regulation range of the dc–dc converter output stage by lowering voltage \( V_{BMIN} \). However, because of a strong trade-off between minimum regulation voltage \( V_{BMIN} \) and the conversion efficiency of the dc–dc converter, \( V_{BMIN} \) is usually restricted to 80% to 90% of \( V_{BH} \). With such a selection of \( V_{BMIN} \), only a small part of the energy stored in \( C_B \) is delivered during the hold-up period. The fraction of the delivered energy can be calculated from

\[
\frac{\Delta E_{CB}}{E_{CBH}} = 1 - \left( \frac{V_{BMIN}}{V_{BH}} \right)^2
\]  

where \( \Delta E_{CB} \) is the amount of delivered energy to the output during hold-up time and \( E_{CBH} \) is the total stored energy in \( C_B \) at \( V_{BH} \).

Equation (2) is shown in graphical form in Fig. 2. As seen from Fig. 2, only 19% of the stored energy is delivered to the load during the hold-up time if \( V_{BMIN} \) is selected to be 0.9 \( V_{BH} \). Similarly, if \( V_{BMIN} \) is selected to be 0.8 \( V_{BH} \), 36% of the stored energy is delivered to the output, i.e., the majority of the stored energy is not used to supply the load during hold-up time.

To utilize the majority of the stored energy during hold-up time, \( V_{BMIN} \) must be selected well below 80% of \( V_{BH} \). For example, 75% of the stored energy is delivered to the load for \( V_{BMIN} = 0.5 V_{BH} \). However, with \( V_{BMIN} = 0.5 V_{BH} \), the efficiency of the dc–dc converter and, therefore, the overall efficiency would be severely penalized since the dc–dc converter output stage would be required to operate with a wider input voltage range. Namely, to regulate the output in a wider input voltage range, a wider duty-cycle range is needed, which requires the transformer in the dc–dc converter to have a smaller turns ratio. Generally, a smaller turns ratio increases the primary and, quite often, secondary conduction losses, which deteriorates the conversion efficiency.

### III Optimization of Bulk Energy Utilization

In this paper, a method that substantially improves the utilization of the stored energy in the energy-storage capacitors of a power supply during hold-up time is described. The improvement is achieved by providing two groups of energy storage capacitors, as shown in Fig. 3(a), and by connecting one group of capacitors \( C_{B AUX} \) to the input of a hold-up time extension circuit that has its output connected to another group of energy-storage capacitors \( C_{BO} \). (Each group of energy-storage capacitors may consist of a single capacitor or a number of capacitors connected in parallel.)

The hold-up time extension circuit is designed so that its output is regulated at a voltage that is lower than the minimum regulation voltage of the front-end rectifier. As a result, the hold-up time extension circuit is inactive during normal operation mode, i.e., when the input voltage is present. In fact,
during normal operation mode, both groups of capacitors are effectively connected in parallel so that their voltages are equal.

As shown in Fig. 3(b), the hold-up time extension circuit becomes activated after the line-voltage dropout, which is when the voltage across capacitors $C_{BAUX}$ and $C_{BO}$ discharges to a voltage close to minimum regulation voltage $V_{BMIN}$. Once the hold-up time extension circuit is activated, capacitor $C_{BAUX}$ connected to the input of the hold-up time extension circuit continues to discharge and provide energy to the regulated output of the hold-up time extension circuit. As a result, the voltage across capacitor $C_{BO}$ connected at the output of the hold-up time extension circuit is kept constant at the voltage slightly above minimum regulation voltage $V_{BMIN}$ of the dc–dc converter output stage. Therefore, during this phase of operation, energy stored in the capacitors at the input side of the hold-up time extension circuit is used to deliver the required output power during hold-up time. The hold-up time is terminated when the voltage of capacitor $C_{BAUX}$ at the input side of the hold-up time extension circuit reaches minimum regulation voltage $V_{BMIN}$ of the hold-up time extension circuit. As can be seen from Fig. 3(b), the extension of the hold-up time brought by the hold-up time extension circuit is dependent on the selection of $V_{BAUXMIN}$. A lower $V_{BAUXMIN}$ results in a longer extension of the hold-up time because more energy is taken from capacitor $C_{BAUX}$. For a given $V_{BAUXMIN}$, the extension of the hold-up time depends on

![Fig. 3](image1.png)

Fig. 3 Conceptual implementation of the hold-up time extension circuit: (a) block diagram and (b) energy-storage-capacitor voltage $V_{BO}$ and auxiliary energy-storage-capacitor voltage $V_{BAUX}$ waveforms.

![Fig. 4](image2.png)

Fig. 4. Ratio of the additional discharged energy due to the hold-up time extension circuit $\Delta E_{EC}$ and the discharged energy without the hold-up extension circuit $\Delta E_{CBH}$ as functions of $V_{BMIN}/V_{BH}$ for different $C_{BAUX}/C_{BO}$ ratios: (a) $V_{BMIN}/V_{BH} = 0.9$ and (b) $V_{BMIN}/V_{BH} = 0.8$.

The fraction of energy delivered to the output during the hold-up time with the hold-up time extension circuit is given by

$$\frac{\Delta E_{EC}}{\Delta E_{CBH}} = 1 - \left(\frac{V_{BMIN}}{V_{BH}}\right)^2 \left(\frac{C_{BAUX}}{C_{BO}}\right) \left(\frac{V_{BMIN}}{V_{BH}}\right)^2 \left[1 - \left(\frac{V_{BAUXMIN}}{V_{BMIN}}\right)^2\right]$$

(3)

where total energy storage capacitance $C_{BO}$ is the sum of capacitors $C_{BAUX}$ and $C_{BO}$. The first term on the right-hand side of (3) represents the delivered energy without the hold-up time extension circuit given by (2). The second term represents the additional delivered energy provided by the addition of the hold-up time extension circuit.

To evaluate the effectiveness of the proposed hold-up time extension method, Fig. 4 shows plots of the ratio of the additional discharge energy [second term in (3)] due to hold-up time extension circuit $\Delta E_{EC}$ and the energy discharge without
hold-up time extension circuit $\Delta E_{CB}$ [first term in (3)] as functions of $V_{BAUXMIN}/V_{BH}$ for different $C_{BAUX}/C_B$ ratios. Fig 4(a) presents plots for $V_{BMIN}/V_{BH} = 0.9$, whereas Fig 4(b) shows plots for $V_{BMIN}/V_{BH} = 0.8$, i.e., for the two regulation ranges of the dc-dc converter output stage in Fig 3(a). The plots in Fig 4(a) and (b) are generated by assuming that $C_{BO} + C_{BAUX} = C_B$, i.e., that total energy storage capacitance is the same in the implementations with and without the hold-up time circuit. Therefore, different ratios of $C_{BAUX}/C_B$ used as the parameter in the plots in Fig 4(a) and (b) mean different allocations for the total capacitance $C_B$ among auxiliary capacitance $C_{BAUX}$ and capacitance $C_{BO}$.

As can be seen from Fig 4(a), for a given ratio $V_{BAUXMIN}/V_{BH}$, the amount of extracted energy from the energy-storage capacitors is increased as the ratio $X = C_{BAUX}/C_B$ increases, i.e., as more of the total capacitance is allocated to $C_{BAUX}$. For example, for $V_{BAUXMIN}/V_{BH} = 0.5$ and $X = 0.25$, the hold-up time extension circuit helps extract 74% more energy from the energy-storage capacitors compared to the implementation without the hold-up time extension circuit, which had the same amount of energy-storage capacitance. For larger values of ratio $X = C_{BAUX}/C_B$, the effect of the hold-up time extension circuit is even more dramatic, since it increases the amount of the delivered energy from the storage capacitors by 147% for $X = 0.5$ and 203% for $X = 0.75$.

The effectiveness of the hold-up time extension circuit is also dependent on the regulation range of the dc-dc converter in Fig 3(a), i.e., it is dependent on the $V_{BMIN}/V_{BH}$ ratio. As can be seen from Fig 4(b), for $V_{BMIN}/V_{BH} = 0.8$ and $V_{BAUXMIN}/V_{BH} = 0.5$, the hold-up time extension circuit helps extract 27%, 54%, and 81% more energy for $X = 0.25$, $X = 0.5$, and $X = 0.75$, respectively.

The improved utilization of the stored energy in the energy-storage capacitors makes it possible to optimize the circuit performance by meeting the hold-up time requirement with minimal energy-storage capacitance.

Generally, for maximum effectiveness of the hold-up time circuit, it is necessary to maximize auxiliary capacitance $C_{BAUX}$ since the energy stored in $C_{BAUX}$ is delivered to the output when the hold-up time extension circuit is activated. The energy stored in capacitor $C_{BO}$ is only delivered during the hold-up time period before the hold-up time extension circuit is activated at approximately $V_{BMIN}$. Therefore, the optimal design of the hold-up time extension circuit requires that the available total energy-storage capacitance be allocated between $C_{BO}$ and $C_{BAUX}$ so that $C_{BAUX}$ is maximized. In practice, this allocation is usually dictated by minimum capacitance $C_{BO}$, which handles the voltage and current ripple produced at the output of the hold-up time extension circuit.

### IV Hold-Up Time Extension Circuit with Integrated Magnetics

The hold-up time extension circuit can be simply implemented with any boost-like topology, i.e., with any nonisolated or isolated topology that can operate with its output voltage greater than its input voltage. Fig 5 shows a power supply with a boost PFC front end and an implementation of the hold-up time extension circuit that uses the boost topology.

The major disadvantage of the proposed circuit shown in Fig 5 is the addition of the components for the hold-up time extension circuit. That may degrade power density improvement by reducing the size of the energy storage capacitors for the same hold-up time requirements. To minimize the additional volume, switch $S_{AUX}$ and diode $D_{AUX}$ of the hold-up time extension circuit can be attached to the heat sink of switch $S$ and diodes $D_3$ and $D_6$ of the PFC rectifier since they do not operate at the same time. Moreover, inductor $L_{AUX}$ can be integrated into boost inductor $L$ to maximize the utilization of the magnetic cores. It should be noted that diode $D_6$ doesn’t need to be a fast rectifier.

Fig 6 shows the proposed integrated magnetic device with decoupled energy storage and its symbol. The proposed magnetic device employs two windings and two toroidal cores. The first winding consists of windings $N_{A1}$ and $N_{A2}$ connected in series. Second winding $N_{B1}$ is wound around both cores, as shown in Fig 6. Winding $N_{A1}$ is wound on the first core in the same direction as winding $N_{B1}$. However, winding $N_{A2}$ is wound on the second core in the opposite direction of winding $N_{B1}$. The simplified electrical model of the integrated magnetic device is also shown in Fig 6.

To facilitate the explanation of the device, Fig 7 shows the integrated magnetic device in Fig 6 with referenced directions of currents and magnetic fluxes as current $i_A$ flows through winding $N_{A1} - N_{A2}$. To make the windings magnetically independent from each other, winding $N_{A1}$ and winding $N_{A2}$ should have an equal number of turns, i.e., $N_{A1} = N_{A2} = N_A$. As can be seen in Fig 7, current $i_A$ generates magnetic flux $\phi_A = N_A \times i_A/R$ in the first and second cores in opposite directions, where $R$ is the reluctance of the magnetic path in the cores. Because of the flux directions, the overall flux encircled by winding $N_{B1}$ is zero, and hence, the induced current in winding $N_{B1}$ is also zero, i.e., $i_{B1} = 0$.

Fig 8 shows the integrated magnetic device in Fig 6 with referenced directions of currents and magnetic fluxes as current $i_B$ flows through winding $N_{B1}$. Current $i_B$ generates magnetic flux $\phi_{B1} = N_{B1} \times i_B/R$ in the first and second cores, which
Fig. 6. Two-winding integrated magnetic device with the decoupled energy storage and its simplified symbol.

Fig. 7. Integrated magnetic device in Fig. 6 with reference directions of currents and magnetic flux as current $i_A$ flows through winding $N_{A1} - N_{A2}$.

The change of flux $\phi_{B1}$ induces the current in windings $N_{A1}$ and $N_{A2}$. Because of the winding directions and the equal number of turns of $N_{A1}$ and $N_{A2}$, the induced currents in windings $N_{A1}$ and $N_{A2}$ are opposite and cancel to be zero, i.e., $i_A = 0$. Moreover, induced voltage $V_{N_A}$ across the first winding is not influenced by current $i_B$ in the second winding because voltage $V_{N_A}$ is proportional to the varying rate of current $i_A$, which is zero. As a result, the first winding and the second winding are magnetically independent, and can be used as two different inductors. Fig. 9 shows the hold-up time extension circuit with the proposed integrated magnetic device.

Fig. 8. Integrated magnetic device in Fig. 6 with reference directions of currents and magnetic flux as current $i_B$ flows through winding $N_{B1}$.

Fig. 9. Hold-up time extension circuit and front-end PFC rectifier with the two-winding integrated magnetic device.

Fig. 10. Windings $N_{A1}$ and $N_{A2}$ of the integrated magnetic device. Triple insulated wires are used.
V EXPERIMENTAL RESULTS

The performance of the proposed hold-up time extension circuit, which is shown in Fig. 9, was verified on a 1-kW prototype circuit that was designed to operate from a 90–264 V ac input range and deliver 12 V of dc output voltage. The experimental circuit was implemented with the following components: switch $S_{\text{AUX}}$-IR4PC50W, diodes $D$, $D_{\text{AUX}}$, $D_{\text{AUX}}$-RHRP1560; capacitor $C_{\text{BO}}$ - 180 $\mu$F/450 V; and capacitor $C_{\text{BAUX}}$ - 2 x 650 $\mu$F/450 V. Switch $S_{\text{AUX}}$ and diode $D_{\text{AUX}}$ of the hold-up time extension circuit were attached to the heat sink for switch $S$ and diode $D$ of the PFC rectifier since they do not operate at the same time. The structure of the integrated magnetic device is shown in Figs. 10 and 11. The cores of integrated inductor $L_{\text{AUX}}$ are MS-130-060. Triple insulated wires (40 turns, O.D 0.5 mm) were used for windings $N_{A1}$ and $N_{A2}$. A magnet wire (70 turns, AWG# 16) was used for winding $N_{B1}$. The measured voltage gain between windings $N_{A1}$-$N_{A2}$ and $N_{B1}$ was approximately -60 dB. A constant-frequency voltage-mode PWM controller was utilized for the hold-up time extension circuit. The required space for the proposed hold-up time extension circuit is less than 1% of the overall volume of the power supply.

Fig. 12(a) and (b) show the measured waveforms of the converter with and without the proposed hold-up time extension circuit, respectively. The current through inductor $L_{\text{AUX}}$ of the hold-up time extension circuit is shown in Fig. 12(c). As shown in Fig. 12, the hold-up time is extended from approximately 24 to 87 ms with the proposed hold-up time extension circuit that utilizes bulk capacitors of the same size.

VI. CONCLUSION

A circuit that substantially improves the utilization of the bulk capacitor energy during hold-up time has been introduced. By employing integrated magnetics approach, the volume of the additional circuitry required to extend the hold-up time is minimized. In a 1-kW prototype circuit used to verify the operation and performance of the proposed approach, the hold-up time was extended from approximately 24 to 87 ms using the same total bulk capacitance. The volume of additional components that were used to implement the hold-up-time extension circuit were less than 1% of the overall volume of the prototype.

REFERENCES

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