

Implementation and Performance Evaluation of DSP-Based Control for Constant-Frequency Discontinuous-Conduction-Mode Boost PFC Front End

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Abstract—A digital signal processor (DSP) implementation of digital control for constant-frequency, discontinuous-conduction-mode boost power-factor-correction converter for universal line-voltage (90–264 V_{rms}) applications is presented. A step-by-step design procedure based on digital redesign technique is also provided. The performance evaluation of the proposed DSP control is performed on a 400-W prototype. It was shown that the implemented DSP-based control can achieve a power factor higher than 0.99 in the entire line range.

Index Terms—Boost, constant frequency, control, discontinuous conduction mode (DCM), power-factor correction (PFC).

I. INTRODUCTION

UNTIL recently, the application of the digital control of switch-mode power conversion circuits was limited to motor drives (MDs), uninterruptible power supplies (UPSs), and three-phase, telecom switch-mode rectifiers (SMRs). The other switch-mode power supplies (SMPSs) have been exclusively designed with analog control due to its low cost and ability to achieve a tight voltage regulation in the presence of fast input voltage and load changes. However, with the emergence of high-speed and relatively low-cost digital signal processors (DSPs), micro controllers (μ Cs), and field-programmable gate arrays (FPGAs), the implementation of digital control in a broad range of SMPSs has become feasible. In fact, interest in applying digital technology to the next generation of SMPSs has significantly risen since DSP-based control offers many features that are not found in analog control such as, for example, programmability, flexibility, insensitivity to aging and environmental variations (e.g., temperature and humidity), intelligence (e.g., self-diagnosis, parameter estimations, etc.), and real-time communications. In addition, digital control is particularly suited for implementing sophisticated control algorithms such as nonlinear control, fuzzy logic control, and adaptive control. Finally, the implementation of soft-start control and management of fault protection is far more flexible and often simpler in digital-based control than in its analog

counterpart, especially when communication between power supply and the rest of the system is required.

A distinct advantage to today's DSP's over their predecessors is that current instruction speeds and analog-to-digital converter (ADC) conversion rates are fast enough compared to the control-loop bandwidths of the majority of today's power converters so that the DSP-based digital control can deliver a satisfactory performance. For example, simple, low-cost state-machine-based digital controllers have already been commercially available for applications in voltage regulation modules (VRMs) [1] and flyback converters [2]. In addition, the results of intensified R&D activities in applying digital control to single-phase power-factor-correction (PFC) circuits and dc-dc converters using DSP-based control have been reported recently [3]–[11].

Generally, PFC converters are the most suitable for digital control implementation because they require control loops with relatively low bandwidths. Specifically, in the continuous-conduction-mode (CCM) boost PFC converter, the current loop bandwidth is typically below 5 kHz, whereas the voltage-loop bandwidth is well below 100 Hz. The digital-based control implementation of the discontinuous-conduction-mode (DCM) boost PFC is even simpler since only a low-bandwidth voltage loop is necessary for the control of the DCM boost PFC converter.

This paper presents a design of a DSP-based digital control for a 400-W 100-kHz, constant-frequency DCM boost PFC converter module for universal-input voltage range (90–264 V_{rms}). The DCM boost PFC converter topology is selected due to its simplicity and good performance. Generally, in the DCM boost converter the reverse-recovery-related losses of the fast-recovery boost diode are eliminated because the boost diode current becomes zero before a reverse voltage is applied across the diode. Also, the DCM boost PFC converter can be implemented with a smaller size boost inductor compared to its CCM counterpart. In addition, the DCM boost PFC converter control implementation does not require current sensing, i.e., the control can be implemented with the voltage-feedback loop only. Finally, interleaving of constant-frequency DCM boost PFC modules to obtain a higher power PFC front end is significantly easier to achieve than CCM due to DCMs' inherent current sharing between modules. Furthermore, since a DSP is often supplied with multiple timers, phase shifting of switching period is trivial compared to analog control [10].

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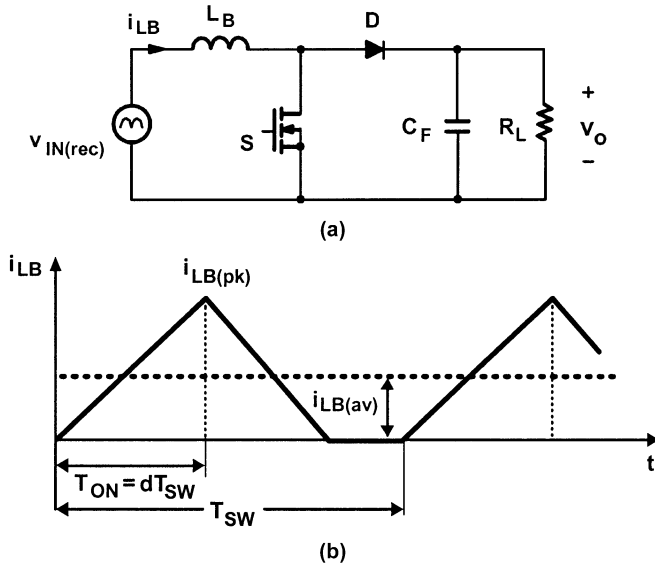


Fig. 1. Boost converter. (a) Power stage. (b) Inductor-current waveform in DCM.

II. CONTROL STRATEGIES FOR DCM BOOST PFC CONVERTER

The circuit diagram of the constant-frequency DCM boost PFC converter and its typical inductor (rectified input) current waveform are shown in Fig. 1. From Fig. 1(a), peak inductor current $i_{LB(pk)}$ can be calculated as

$$\begin{aligned} i_{LB(pk)} &= \frac{v_{IN(rec)}}{L_B} \cdot T_{ON} = \frac{|V_M \sin \omega_L t|}{L_B} \cdot T_{ON} \\ &= \frac{|V_M \sin \omega_L t|}{L_B} \cdot d \cdot T_{SW} \end{aligned} \quad (1)$$

where $v_{IN(rec)}$ is the rectified line voltage, L_B is the inductance of the boost inductor, T_{ON} is the on time of boost switch S , V_M is the magnitude of the input (line) voltage, ω_L is the line frequency, d is the duty cycle, and T_{SW} is the switching period.

According to (1), if on time T_{ON} , i.e., duty cycle d , is kept constant over a half line period $T_L/2$, peak boost-inductor current $i_{LB(pk)}$ is sinusoidal. However, the boost-inductor current averaged over a switching period, $i_{LB(av)}$, which represents the line current, is distorted since from Fig. 1(a) it can be easily derived as

$$i_{LB(av)} = \frac{d^2 \cdot T_{SW}}{2L_B} \cdot \frac{v_O}{v_O - v_{IN(rec)}} \cdot v_{IN(rec)} \quad (2)$$

where v_O is the output voltage.

The distortion factor in (2)

$$\frac{v_O}{v_O - v_{IN(rec)}} = \frac{1}{1 - \frac{v_{IN(rec)}}{v_O}} \quad (3)$$

depends on the ratio of the peak line voltage and output voltage. Generally, the line current distortion decreases as the difference between output voltage v_O and peak line voltage V_M increases, i.e., as their ratio becomes higher. Therefore, the maximum distortion occurs at the maximum line voltage [12].

Generally, the control of the DCM boost PFC converter is implemented by single-loop feedback control that regulates output voltage v_O . In such a control, a constant duty cycle that is required to obtain PFC function is achieved by designing the bandwidth of the control loop well below the rectified frequency of the line, i.e., by keeping the bandwidth well below 100 Hz. Typically, the bandwidth of the control loop of the DCM boost PFC converter designed for universal input voltage range is around 5–15 Hz.

Despite the increased line current distortions, the constant-frequency DCM boost PFC converter operated with constant duty-cycle control can meet the EN-61000-3-2 harmonic-limit specifications (mandated in the European Union countries) and the corresponding voluntary Japanese harmonic-limit specifications with plenty of margin. However, the power factor for European line voltages, i.e., for nominal voltages in the 220–240- V_{rms} range, cannot exceed approximately 0.95. On the other hand, the power factor for Japanese and U.S. line voltages (nominal voltage range 100–115 V_{rms}) of over 0.99 can be achieved. Although, EN-61000-3-2 and the corresponding Japanese specification do not specify the limits on power factor, many electronic equipment manufacturers have their internal specs which require a power factor greater than 0.98 to be maintained over the entire universal-line range (90–264 V_{rms}). As a result, the DCM boost PFC converter with the constant duty-cycle (on-time) control cannot be used in applications that require a power factor of more than 0.95 for European line voltages.

The performance of the constant-frequency DCM boost PFC converter can be significantly improved by employing the variable duty-cycle control as described in [13]–[15]. Namely, as can be seen from (2), average inductor current $i_{LB(av)}$ that represents the rectified line current will perfectly follow rectified line voltage $v_{IN(rec)}$ if the term

$$d^2 \cdot \frac{v_O}{v_O - v_{IN(rec)}} = \lambda = \text{const.} \quad (4)$$

is kept constant during a half line cycle, i.e., if the duty-cycle is modulated as

$$d = \sqrt{\lambda} \cdot \sqrt{1 - \frac{v_{IN(rec)}}{v_O}}. \quad (5)$$

With the duty-cycle modulation strategy given in (5), the line current distortions are virtually independent of the line voltage and are very much reduced compared to those for constant duty-cycle control, especially for the European power-line range (180–264 V_{rms}). In addition, this type of control makes it possible to maintain a power factor greater than 0.99 over the entire universal-line range (90–264 V_{rms}).

A number of analog implementations of the control law in (5) were introduced and described in [13]–[15]. Generally, these implementations require sensing of both the output and input voltages and the use of either analog multipliers [13], [14], or two resettable integrators [15]. The DSP implementation of the control law in (5) is much easier since square root, multiplication, and subtraction operation that are required in (5) can be easily programmed into a DSP.

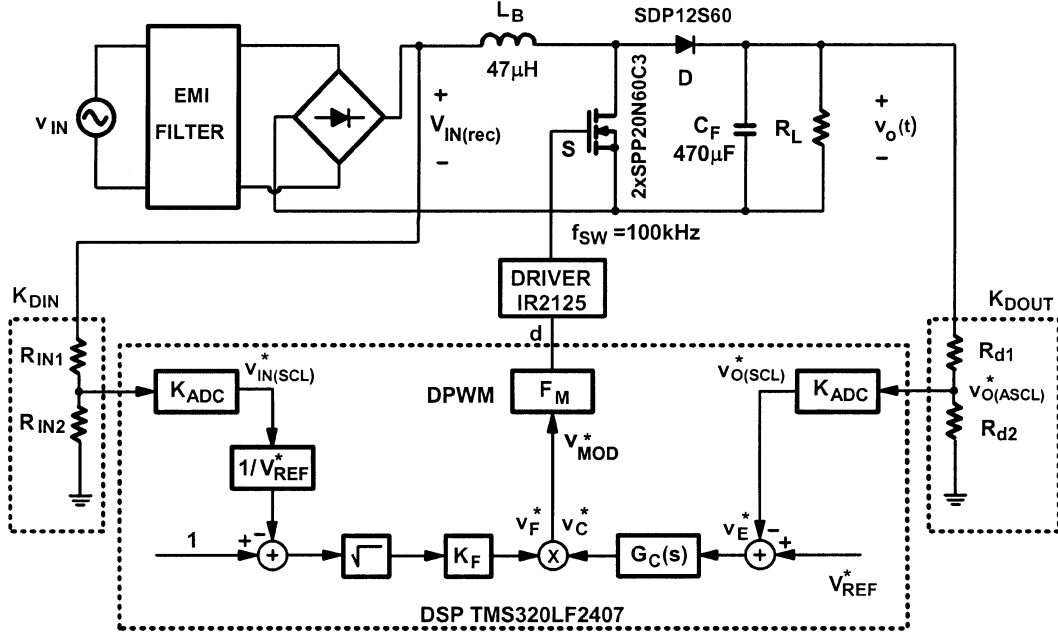


Fig. 2. Simplified diagram of DSP-based digital control of constant-frequency DCM boost PFC converter.

III. DIGITAL CONTROL IMPLEMENTATION

A simplified diagram of a digitally controlled constant-frequency DCM boost PFC converter is shown in Fig. 2. The power stage component values indicated in Fig. 2 correspond to a 100-kHz DCM boost PFC prototype module that can deliver 400 W from a 385-V output in the entire universal line-voltage range $V_{IN} = 90\text{--}264 V_{\text{rms}}$.

As can be seen from Fig. 2, in the implementation of the variable duty-cycle control, both the input and output voltages are sensed. The sensed voltages are scaled down and then sampled and digitized by the ADCs for further processing by DSP. Note that in Fig. 2, the star (*) notation is used to denote digitized quantities. Digitized scaled input voltage $v_{IN(SCL)}^*$ is further processed to obtain feedforward signal v_F^* . Similarly, digitized output voltage $v_{O(SCL)}^*$ is processed by the error-amplifier in the output-voltage control loop to generate control signal v_C^* . Finally, feedforward signal v_F^* and control-voltage signal v_C^* are multiplied and the resultant signal v_{MOD}^* is fed to the input of the digital pulsewidth-modulation modulator (DPWM) with a gain of F_M to generate the desired duty cycle.

From Fig. 2, voltage v_F^* is given by

$$\begin{aligned} v_F^* &= K_F \sqrt{1 - \frac{v_{IN(SCL)}^*}{V_{REF}^*}} \\ &= K_F \sqrt{1 - \frac{(K_{DIN} \cdot K_{ADC} \cdot v_{IN(rec)})^*}{V_{REF}^*}} \end{aligned} \quad (6)$$

where K_F is the scaling gain of the feedforward signal, V_{REF}^* is the reference voltage, K_{DIN} is the gain of the rectified-line voltage divider, and K_{ADC} is the gain of ADC.

Since for a properly designed output-voltage regulation loop

$$V_{REF}^* \approx v_{O(SCL)}^* = (K_{DOUT} \cdot K_{ADC} \cdot v_O)^* \quad (7)$$

where K_{DOUT} is the gain of output-voltage divider, voltage v_F^* is

$$\begin{aligned} v_F^* &\approx K_F \sqrt{1 - \frac{v_{IN(SCL)}^*}{v_{O(SCL)}^*}} \\ &= K_F \sqrt{1 - \frac{(K_{DIN} \cdot K_{ADC} \cdot v_{IN(rec)})^*}{(K_{DOUT} \cdot K_{ADC} \cdot v_O)^*}} \\ &= K_F \sqrt{1 - \frac{v_{IN(rec)}^*}{v_O^*}} \end{aligned} \quad (8)$$

if $K_{DIN} = K_{DOUT}$.

The duty cycle d in the digital control implementation in Fig. 2 is given by

$$\begin{aligned} d &= v_F^* \cdot v_C^* \cdot F_M = K_F \cdot v_C^* \cdot F_M \sqrt{1 - \frac{v_{IN(rec)}^*}{v_O^*}} \\ &= K_F \cdot v_C^* \cdot F_M \sqrt{1 - \frac{v_{IN(SCL)}^*}{v_{O(SCL)}^*}} \end{aligned} \quad (9)$$

which is exactly the same as the control law described in (5) if term $K_F \cdot v_C^* \cdot F_M$ is made constant during a half line cycle, i.e., if

$$K_F \cdot v_C^* \cdot F_M = \sqrt{\lambda} = \text{const.} \quad (10)$$

To make the product in (10) constant, control voltage v_C^* has to be constant. The control voltage can be made approximately constant if the control loop bandwidth is kept well below the rectified line frequency of 100 Hz. It should be noted that a second-harmonic ripple exists in the output voltage, which will make the approximation of the digitized output voltage with the constant reference voltage that is given by (7) less accurate. To

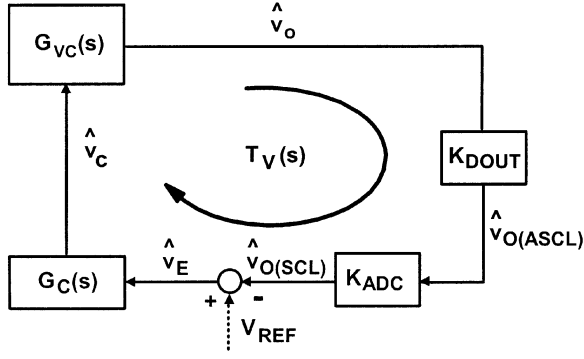


Fig. 3. Control block diagram of DCM boost PFC converter.

minimize the line-current distortion due to a reduced accuracy in calculating the required duty cycle, the output voltage ripple should be small. In practice, the value of the energy-storage capacitor at the output of the PFC converter that is determined by the hold-up time requirement is usually large enough to keep the output voltage ripple small so that the ripple does not have significant effect on the current distortion.

A. Controller Design

Generally, if the sampling frequency of a digital controller is selected to be much higher than the control-loop bandwidth, the design of the digital controller can be performed in the analog domain (s domain) and then translated into the digital domain. This approach, known as the digital redesign approach is taken in the design of the digital controller in Fig. 2 since the selected sampling frequency $f_S = 100$ kHz is much greater than the output-voltage control-loop bandwidth that is well below 100 Hz. With a sampling frequency more than four decades higher than the loop bandwidth, the digital redesign approach can be applied with good accuracy.

The s -domain block diagram of the digitally controlled DCM boost PFC converter in Fig. 2 is shown in Fig. 3, where block $G_{VC} = \hat{v}_O/\hat{v}_C$ is the small-signal control-to-output transfer function of the constant-frequency DCM boost PFC converter with feedforward path closed. It should be noted that in the block diagram in Fig. 3, the effect of the ADC conversion time and DSP computation time on the control loop phase margin is neglected since these two delays combined are much shorter than one sampling period, i.e., $10 \mu\text{s}$, which, virtually, does not produce any phase delay at a crossover frequency below 100 Hz.

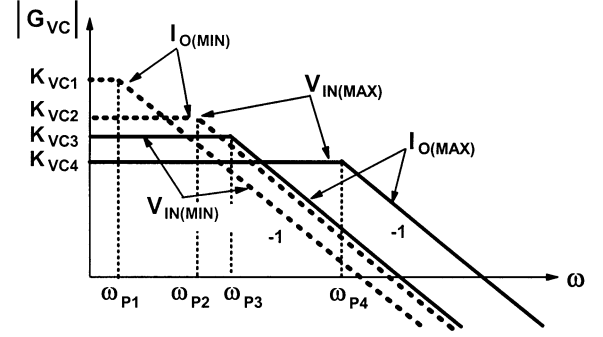
From Fig. 3, loop gain $T_V(s)$ is given by

$$T_V(s) = K_{DOUT} \cdot K_{ADC} \cdot G_C(s) \cdot G_{VC}(s). \quad (11)$$

To design compensator $G_C(s)$, it is necessary to know small-signal control-to-output transfer function G_{VC} and values of constant gains K_{DOUT} and K_{ADC} .

1) *Small-Signal Transfer Function $G_{VC}(s)$* : As derived in [14], small-signal control-to-output transfer function G_{VC} of the variable-duty cycle constant-frequency DCM boost PFC for constant resistance load is

$$G_{VC}(s) = K_{VC} \frac{1}{1 + \frac{s}{\omega_P}} \quad (12)$$


 Fig. 4. Asymptotic magnitude Bode plots of control-to-output transfer function G_{VC} for different operating conditions.

where

$$K_{VC} = \frac{V_M \cdot K_F \cdot F_M}{2 \cdot \bar{f} + 1} \cdot \sqrt{\frac{R_L}{L_B \cdot f_{SW}}} \quad (13a)$$

$$\omega_P = 2\pi f_P = \frac{2 \cdot \bar{f} + 1}{C_F R_L} \quad (13b)$$

$$\bar{f} = \frac{M_P^3}{\sqrt{M_P^2 - 1}} \left[1 + \frac{2}{\pi} \sin^{-1} \frac{1}{M_P} \right] - M_P^2 - \frac{2}{\pi} M_P \quad (13c)$$

and

$$M_P = \frac{v_O}{V_M} \quad (13d)$$

where V_M is the magnitude (peak) of the line voltage, f_{SW} is the switching frequency, L_B is the inductance of the boost inductor, and R_L is the load resistance.

Dc gain K_{VC} and pole frequency ω_P of single-order transfer function $G_{VC}(s)$ are dependent on the line voltage and load current (resistance), as illustrated in Fig. 4, which shows asymptotic Bode plots of the G_{VC} magnitude.

To calculate gain K_{VC} , it is necessary to know gain F_M of the digital PWM modulator.

2) *Digital Modulator Gain F_M* : With today's DSPs, various implementations of the modulator are possible depending on the available DSP features. In this development, an approach that employs a counter and a digital comparator, as illustrated in Fig. 5(a), was taken.

The modulator generates duty cycle d by counting clock periods T_{CLK} and by comparing the counter content with the binary representation of control signal v_{MOD}^* . At the beginning of each switching period T_{SW} the counter is reset to zero and the output of the comparator is set high since the binary number representing signal v_{MOD}^* is larger than the up-counter content, as shown in Fig. 5(b). When the counter number reaches the number representing control signal v_{MOD}^* , the output of the digital comparator changes state, i.e., it makes a transition from high to low.

According to the waveform in Fig. 5(b), modulator gain F_M is given by

$$F_M = \frac{\hat{d}}{\hat{v}_{MOD}^*} = \frac{1}{N_{PER}} \quad (14)$$

where N_{PER} is the maximal count of the counter.

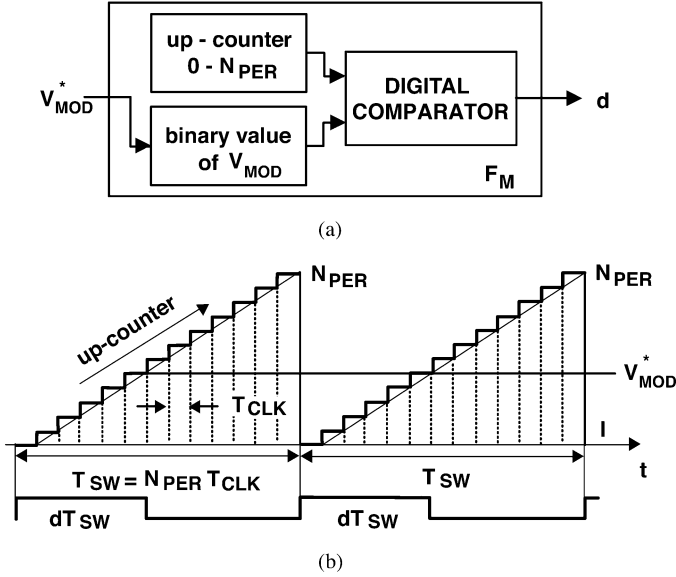


Fig. 5. Digital PWM: (a) conceptual implementation, (b) illustration of operation.

Because the value of N_{PER} is determined by switching period T_{SW} and clock period T_{CLK} , as shown in Fig. 5(b),

$$T_{SW} = N_{PER} \cdot T_{CLK} \quad (15)$$

the modulator gain is given by

$$F_M = \frac{1}{N_{PER}} = \frac{f_{SW}}{f_{CLK}}. \quad (16)$$

3) *Output Voltage Scaling Gain K_{DOUT}* : To ensure that a voltage of the proper magnitude is applied to the ADC, the output voltage of the converter must be scaled down. According to Fig. 3, output-voltage scaling gain K_{DOUT} is given by

$$K_{DOUT} = \frac{v_{O(ASCL)}}{v_O}. \quad (17)$$

To maximize the ADC conversion accuracy, it is better to utilize the full-scale range of the ADC output. Generally, the full-scale range of the ADC output is obtained when the ADC input is equal to ADC's reference voltage V_R . Therefore, scaling gain K_{DOUT} should be determined so that analog scaled output voltage $V_{O(ASCL)}$ reaches its full-scale value V_R when output voltage v_O is maximal. Assuming that the overvoltage protection (OVP) set point is 15% above nominal voltage v_O and with an additional 10% design margin, sensing gain K_{DOUT} can be calculated from

$$V_{O(ASCL)} = V_R = K_{DOUT}(1.25 \cdot v_O) \quad (18)$$

i.e.,

$$K_{DOUT} = \frac{V_R}{1.25 \cdot v_O} = \frac{0.8 \cdot V_R}{v_O}. \quad (19)$$

V_R is the internal reference of the ADC. For example, for the embedded ADC in TI's DSP TMS320LF2704A, reference voltage $V_R = 3.3$ V.

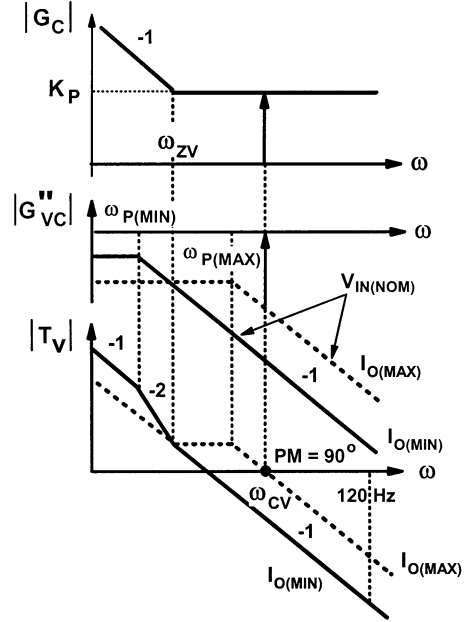


Fig. 6. Controller compensation design.

4) *ADC Gain K_{ADC}* : The ADC converts scaled output voltage $v_{O(ASCL)}$ into binary number $v_{O(SCL)}^*$ which is processed by the DSP. Assuming that the full-scale binary word at the output of ADC represents number 1, i.e., assuming that when the input voltage to the ADC is equal to the ADC's reference voltage V_R the output binary number represents number 1, the gain of ADC is given by

$$K_{ADC} = \frac{v_{O(SCL)}}{v_{O(ASCL)}} = \frac{1}{V_R}. \quad (20)$$

It should be noted that in this DSP-based control, gain K_{DOUT} is not determined from the requirement to make the output voltage in compliance with reference voltage V_{REF}^* as in the case of analog control, but gain K_{DOUT} is determined from the full-scale range requirement of the ADC. As a result, the digital reference V_{REF}^* in Fig. 2 that is generated by the DSP cannot be selected arbitrarily. Namely, according to Fig. 6 once gains K_{ADC} and K_{DOUT} are determined, digital reference V_{REF}^* required to regulate (nominal) output voltage v_O must be equal to the output of the ADC converter at nominal output voltage v_O , i.e.,

$$V_{REF}^* = K_{ADC} \cdot K_{DOUT} \cdot v_O = \frac{1}{V_R} \cdot \frac{0.8 \cdot V_R}{v_O} \cdot v_O = 0.8. \quad (21)$$

B. Compensator Design in s Domain

Generally, the selection of the controller type and its compensation is based on the requirement that loop gain $T_V(s)$ given by (11) is stable with acceptable phase margin (typically, $PM > 45^\circ$) in the entire line-voltage and load-current range, has high low-frequency gain to meet regulation accuracy specifications, and has specified bandwidth.

Since control-to-output-transfer function $G_{VC}(s)$ is a single-pole transfer function, as illustrated in Fig. 4, to obtain a high

loop gain at low frequencies and achieve desired regulation accuracy, it is necessary to use a proportional and integral (PI) controller

$$G_C(s) = K_P + \frac{K_I}{s} = K_P \cdot \frac{s + \omega_{ZV}}{s} \quad (22)$$

where compensator zero $\omega_{ZV} = 2\pi f_{ZV}$ is

$$\omega_{ZV} = \frac{K_I}{K_P}. \quad (23)$$

Because dc gain K_{VC} and pole frequency ω_P of transfer function $G_{VC}(s)$ depend on the line voltage and output load current (power), the loop compensation must be performed in worst case so that loop stability and a proper loop bandwidth are ensured over the entire operating range. The worst-case design requires that the compensation is calculated based on the maximum line voltage $V_{IN(MAX)} = 264 \text{ V}_{\text{rms}}$ and minimum load current $I_{O(MIN)}$. However, for such compensation, the loop bandwidth at minimum line voltage $V_{IN(MIN)} = 90 \text{ V}_{\text{rms}}$ would be very much reduced since gain K_{VC} at the minimum line is much lower than at the maximum line. This would significantly deteriorate the transient response of the converter operating off the 115- V_{rms} power line (Japanese/U.S. power line).

For a universal line-voltage PFC front end, a DSP-based control offers the opportunity to virtually eliminate the variations of the bandwidth with the line voltage. Namely, in a DSP-based control it is trivial to implement two sets of controller parameters, one that is optimized for the European line-voltage range (nominal voltage $V_{IN(NOM)} = 220 \text{ V}_{\text{rms}} \pm 20\%$) and the other that is optimized for Japanese/U.S. line-voltage range ($V_{IN(NOM)} = 115 \text{ V}_{\text{rms}} \pm 20\%$). Since in the control shown in Fig. 2 the rectified line voltage is sensed, the controller has the information about the line voltage so it can execute the appropriate control algorithm.

Furthermore, once the controller design is separated into two narrow-line-range designs, the 20% variation of the line voltage around the nominal line voltage can be neglected since it translates to a variation of less than 3 dB. Therefore, for each line-voltage range the compensator optimization can be performed based on nominal line voltage $V_{IN(NOM)}$ and minimum load current $I_{O(MIN)}$.

To maintain good phase margin over the entire load range, PI-controller zero ω_{ZV} should be placed at approximately 1–2 octaves above the frequency of minimum-load pole $\omega_{P(MIN)}$ [14], i.e., at a frequency that is two-to-four times higher than $\omega_{P(MIN)}$. In this design, the PI-controller zero ω_{ZV} is placed at

$$\omega_{ZV} = 3 \cdot \omega_{P(MIN)} \quad (24)$$

as illustrated in the asymptotic magnitude Bode plots in Fig. 6. Note that in Fig. 6, transfer function $G''_{VC}(s) = K_{DOUT} \cdot K_{ADC} \cdot G_{VC}(s)$, i.e., it has the same corner frequency as $G_{VC}(s)$ since gains K_{DOUT} and K_{ADC} are not dependent on frequency.

Proportional gain K_P of the controller is determined from the condition that loop gain T_V at full load $I_{O(MAX)}$ is unity at crossover frequency ω_{CV} , i.e.,

$$\left| T_V^{\text{MAX}}(j\omega_{CV}) \right| = \left| K_{VC(MAX)} \frac{1}{1 + j\omega_{CV}/\omega_{P(MAX)}} \cdot K_{DOUT} \cdot K_{ADC} \cdot K_P \frac{j\omega_{CV} + \omega_{ZV}}{j\omega_{CV}} \right| = 1 \quad (25)$$

where $K_{V(MAX)}$ and $\omega_{P(MAX)}$ are dc gain and pole frequency of G_{VC} at full load $I_{O(MAX)}$, respectively.

Solving (25), proportional gain K_P of the controller can be obtained as

$$K_P = \frac{\sqrt{1 + \omega_{CV}^2/\omega_{P(MAX)}^2}}{K_{VC(MAX)} K_{DOUT} K_{ADC} \sqrt{1 + \omega_{ZV}^2/\omega_{CV}^2}}. \quad (26)$$

Once compensation zero ω_{ZV} and proportional gain K_P are determined, the integral gain of the controller can be calculated as

$$K_I = \omega_{ZV} K_P. \quad (27)$$

1) *Digital Redesign:* The mapping of the s -domain analog controller $G_C(s)$ into the z -domain ($z = e^{sT_s}$) digital controller $G_C(z)$ can be performed using various mapping functions (transformations). In this development Tustin's transformation is used since it gives better accuracy compared to some other mapping functions. With Tustin's transformation, the digital controller transfer function $G_C(z)$ is obtained as

$$G_C(z) = K_P \cdot \frac{s + \omega_{ZV}}{s} \Big|_{s=\frac{2}{T_s} \cdot \frac{z-1}{z+1}} = \frac{a_0 + a_1 z^{-1}}{1 - z^{-1}} \quad (28)$$

where

$$a_0 = K_P + \frac{K_I T_s}{2} \quad (29)$$

$$a_1 = -K_P + \frac{K_I T_s}{2}. \quad (30)$$

From (28), the recursive relationship between the output of the controller, i.e., control variable $v_C^*(t_n)$, and the input of the controller, i.e., error signal $v_E^*(t_n)$ that is implemented in the DSP is

$$v_C^*(t_n) = v_C^*(t_{n-1}) + a_0 \cdot v_E^*(t_n) + a_1 \cdot v_E^*(t_{n-1}) \quad (31)$$

where t_n and t_{n-1} are the current and immediate previous sampling instants, respectively.

Since the duty cycle of the boost converter is limited to the values between zero and one, the implementation of the PI controller described by (31) may not be able to provide desired transient response to large-signal load and/or line-voltage changes. Namely, if error signal v_E^* is not zero while duty cycle is saturated, the integral part of the controller will continue to change controller output v_C^* to the levels that are far from those required in steady state. As a result, once the duty cycle comes out of the saturation region, the controller output will take longer time to reach the steady-state value, which will worsen the transient response of the control loop.

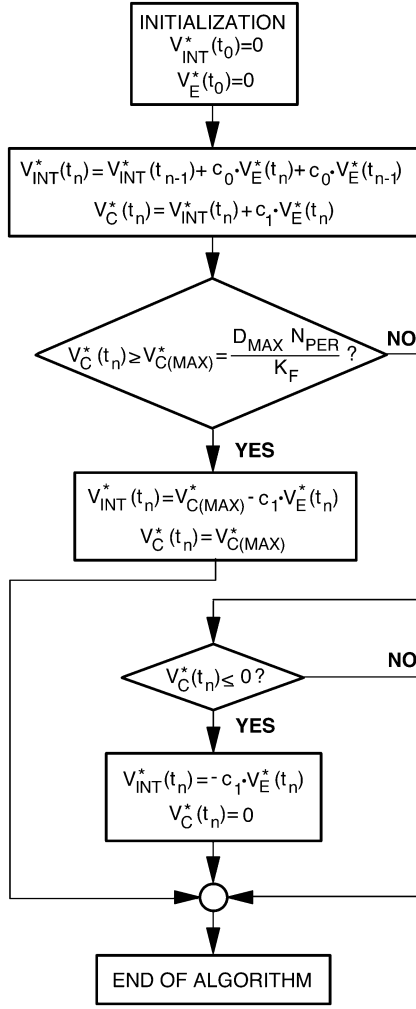


Fig. 7. Flowchart of the PI controller algorithm with antiwindup.

To avoid the PI-controller saturation during transients, the output of the integral part of the controller must be limited, i.e., the PI controller with antiwindup needs to be employed [9]. To implement a digital PI controller with antiwindup, it is necessary to express the controller given in (31) in a form that is represented by the sum of the integral and proportional parts of the controller, i.e., as

$$v_C^*(t_n) = v_{INT}^*(t_n) + c_1 \cdot v_E^*(t_n) \quad (32)$$

and

$$v_{INT}^*(t_n) = v_{INT}^*(t_{n-1}) + c_0 \cdot v_E^*(t_n) + c_0 \cdot v_E^*(t_{n-1}) \quad (33)$$

where

$$c_0 = \frac{K_I T_S}{2} \quad (34)$$

and

$$c_1 = K_P. \quad (35)$$

The implementation of the PI controller algorithm with antiwindup is shown in the flowchart in Fig. 7. In the antiwindup algorithm in Fig. 7, the integral part of the controller is limited by limiting the value of control variable v_C^* between $v_{C(MIN)}^*$ and $v_{C(MAX)}^*$.

Since according to Fig. 2 and (14)

$$v_{MOD}^* = K_F \sqrt{1 - \frac{v_{IN(SCL)}^*}{V_{REF}^*}} \cdot v_C^* = d \cdot N_{PER} \quad (36)$$

and since maximum duty cycle D_{MAX} occurs around zero crossings of the line voltage, i.e., when $v_{IN(rec)} \approx 0$, it follows that

$$v_{C(MAX)}^* = \frac{D_{MAX} \cdot N_{PER}}{K_F}. \quad (37)$$

Similarly, since minimum duty cycle $D_{MIN} = 0$

$$v_{C(MIN)}^* = 0. \quad (38)$$

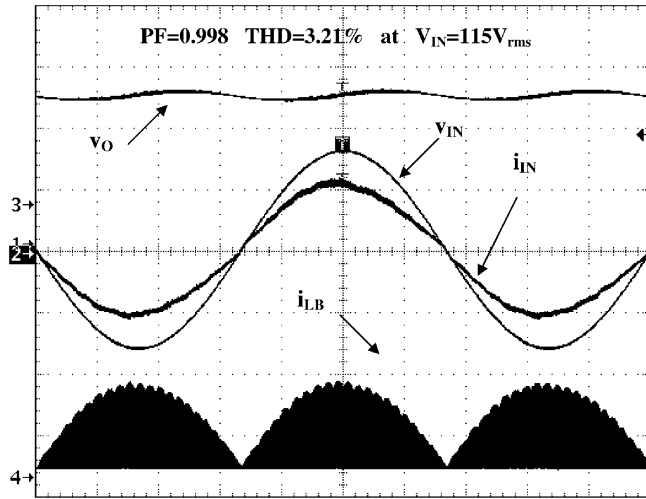
IV. EXPERIMENTAL VERIFICATION

The performance evaluation of the described DSP-based control was verified on a 400-W DCM boost PFC converter designed to operate at constant-switching frequency $f_{SW} = 100$ kHz in the universal line-voltage range $V_{IN} = 90\text{--}264$ V_{rms}. The output voltage of the experimental circuit was regulated at $v_O = 385$ V in the entire load range, i.e., from $I_{O(MAX)} = 1.04$ A (or $R_{L(MIN)} = 370$ Ω) down to $I_{O(MIN)} = 0.1$ A ($R_{L(MAX)} = 3.7$ k Ω). As indicated in Fig. 2, the experimental power stage was built with $L_B = 47$ μ H, and $C_F = 470$ μ F.

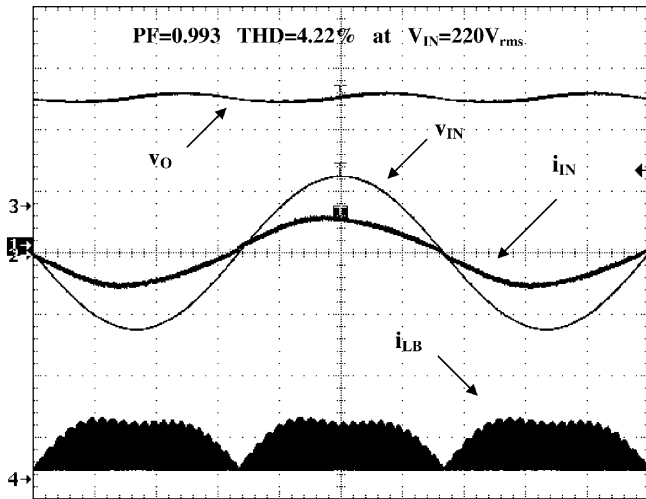
The control was implemented with the fixed-point TMS320LF2407A DSP with a clock frequency of $f_{CLK} = 40$ MHz and sampling rate $f_S = 100$ kHz, which according to (16) gives the DPWM gain of $F_M = 2.5 \cdot 10^{-3}$. Gain of feedforward path $K_F = 400$ was selected in this implementation. The square root operation required to calculate the feedforward signal was implemented by the Taylor series approximation with first seven terms. Since the reference voltage of the embedded ADC's in the TMS320LF2407A is $V_R = 3.3$ V, the output-voltage divider gain determined from (19) is $K_{DOUT} = K_{DIN} = 6.9 \cdot 10^{-3}$, whereas from (20) and (21), the gain of the ADC and the digital reference are $K_{ADC} = 0.3$ and $V_{REF}^* = 0.8$, respectively.

The control-loop bandwidth of the experimental circuit was set to $f_{CV} = 8$ Hz, i.e., $\omega_{CV} = 2\pi f_{CV} = 50$ rad/s for both nominal low-range line voltage $V_{IN(NOM)} = 115$ V_{rms} and nominal high-range line voltage $V_{IN(NOM)} = 220$ V_{rms}. Using (13a), (13b), (24), (26), (27), (34), and (35), the coefficients of the digital PI controller are calculated as $c_0 = 66.8 \cdot 10^{-6}$ and $c_1 = 3.01$ at $V_{IN(NOM)} = 115$ V_{rms} and $c_0 = 68.3 \cdot 10^{-6}$ and $c_1 = 1.69$ at $V_{IN(NOM)} = 220$ V_{rms}.

Fig. 8(a) and (b) shows the measured line-voltage, line-current, boost-inductor current, and output-voltage waveforms of the experimental DCM boost PFC converter with the described variable-duty-cycle digital control at full load and for $V_{IN(NOM)} = 115$ V_{rms} and $V_{IN(NOM)} = 220$ V_{rms}, respectively. As can be seen from the figure, the line current does not exhibit any noticeable distortion at both line voltages. In fact, the measured power factor at both lines is over 0.99, i.e., the total harmonic distortion (THD) is less than 4.5%. For comparison purposes, Fig. 9(a) and (b) shows the corresponding



(a)

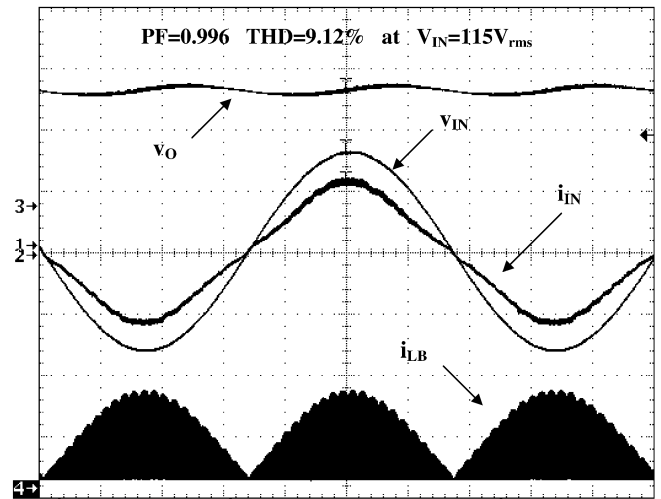


(b)

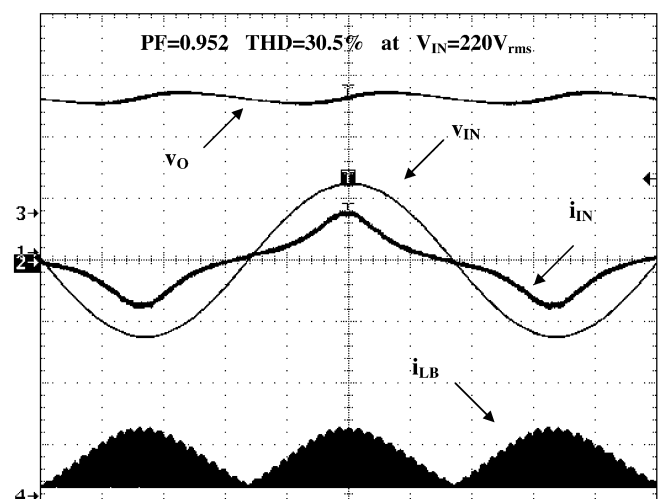
Fig. 8. Measured line voltage v_{IN} , line current i_{IN} , boost-inductor current i_{LB} , and output voltage v_O waveforms with variable-duty-cycle control. (a) Line voltage $V_{IN} = 115 V_{rms}$. (b) Line voltage $V_{IN} = 220 V_{rms}$. i_{IN} : 5 A/div; v_{IN} : 100 V/div in (a) and 250 V/div in (b); v_O : 50 V/div and offset 295 V; i_{LB} : 10 A/div. Time base: 2.5 ms/div.

full-load waveforms for the fixed-duty-cycle implementation (feedforward path removed). As can be seen from Fig. 9(a), at nominal low-line voltage, i.e., $V_{IN(NOM)} = 115 V_{rms}$, the line current is only slightly more distorted compared to that in Fig. 8(a) and the measured power factor is still over 0.99. However, at nominal high-line voltage $V_{IN(NOM)} = 220 V_{rms}$, the line current for the fixed-duty-cycle implementation exhibits severe distortion, as seen in Fig. 9(b) so that the measured power factor is only 0.95.

To illustrate the variable-duty-cycle operation of the DCM boost power stage, Fig. 10 shows blown-up waveforms of boost-switch gate drive signal V_{GS} and boost-inductor current i_{LB} at two instantaneous voltages for full-load operation and $V_{IN(NOM)} = 220 V_{rms}$. As can be seen, the duty cycle of the converter decreases as the input voltage increases, i.e., the duty cycle is larger when the input voltage is 70 V than when the input voltage is 330 V (close to the peak of the line voltage).



(a)



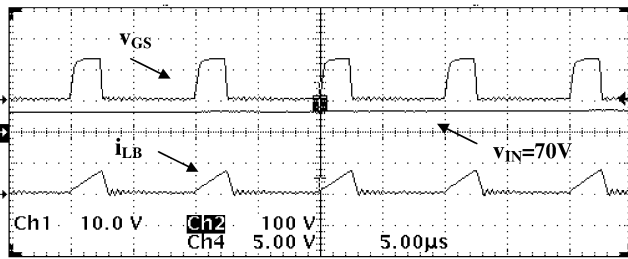
(b)

Fig. 9. Measured line voltage v_{IN} , line current i_{IN} , boost-inductor current i_{LB} , and output voltage v_O waveforms with fixed-duty-cycle control. (a) Line voltage $V_{IN} = 115 V_{rms}$. (b) Line voltage $V_{IN} = 220 V_{rms}$. i_{IN} : 5 A/div; v_{IN} : 100 V/div in (a) and 250 V/div in (b); v_O : 50 V/div and offset 295 V; i_{LB} : 10 A/div. Time base: 2.5 ms/div.

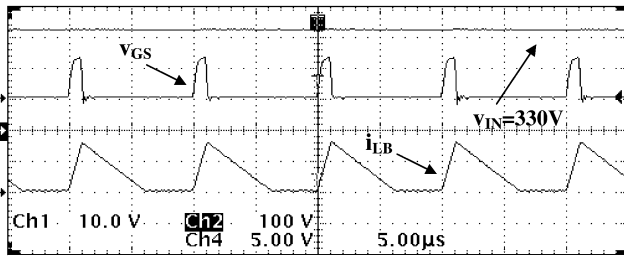
Finally, Figs. 11 and 12 show the full-load-to-no-load step-down and no-load-to-full-load step-up transient responses of the output voltage at $V_{IN(NOM)} = 115 V_{rms}$ and $V_{IN(NOM)} = 220 V_{rms}$, respectively. Because the control algorithm employs two controllers that are optimized to maintain the same bandwidth at $V_{IN(NOM)} = 115 V_{rms}$ and $V_{IN(NOM)} = 220 V_{rms}$, the transient responses at the two lines are almost the same. A slightly smaller output voltage deviation for the step load response at $V_{IN(NOM)} = 220 V_{rms}$ compared to that at $V_{IN(NOM)} = 115 V_{rms}$ can be attributed to a higher low-frequency gain of the control loop at $V_{IN(NOM)} = 220 V_{rms}$.

V. SUMMARY

It has been demonstrated that DSP-based digital control of the universal-line-range constant-frequency DCM boost PFC converter can be implemented with performance that matches that

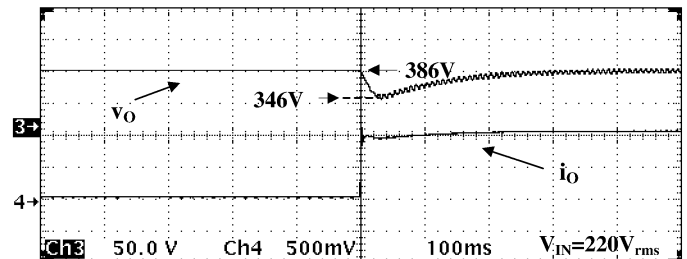


(a)

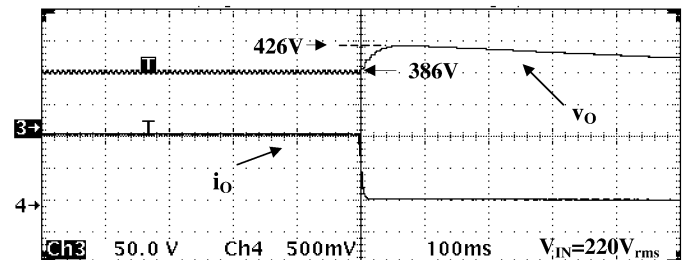


(b)

Fig. 10. Waveforms of boost-switch gate drive signal v_{GS} and boost-inductor current i_{LB} . (a) At instantaneous line voltage $v_{IN} = 70$ V. (b) At instantaneous line voltage $v_{IN} = 330$ V. v_{GS} : 10 V/div; i_{LB} : 5 A/div; v_{IN} : 100 V/div. Time base: 5 μ s/div.



(a)



(b)

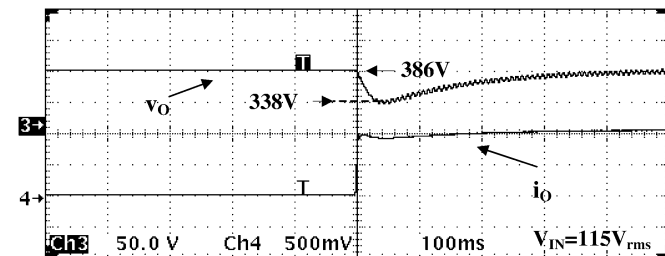
Fig. 12. Waveforms of output current i_O and output voltage v_O for step load-change transients at $V_{IN} = 220$ V_{rms}. (a) No-load-to-full-load step (0–1 A). (b) Full-load-to-no-load step (1–0 A). v_O : 50 V/div and offset 295 V; i_O : 500 mA/div. Time base: 100 ms/div.

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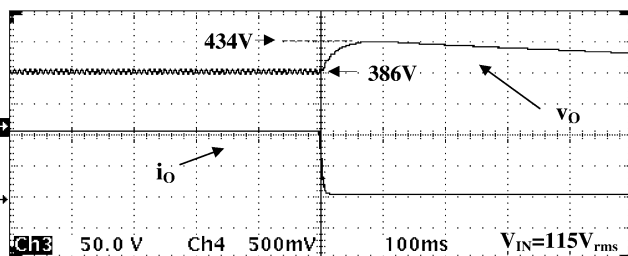
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(a)



(b)

Fig. 11. Waveforms of output current i_O and output voltage v_O for step load-change transients at $V_{IN} = 115$ V_{rms}. (a) No-load-to-full-load step (0–1 A). (b) Full-load-to-no-load step (1–0 A). v_O : 50 V/div and offset 295 V; i_O : 500 mA/div. Time base: 100 ms/div.

of its analog counterpart. In addition to meeting the required harmonic-current limits for both the European and Japanese power lines, the measured power factor of a 400-W experimental prototype was over 0.99 in the entire line and load ranges.



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