

Bridgeless High-Power-Factor Buck Converter

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Abstract—A bridgeless buck power factor correction rectifier that substantially improves efficiency at low line of the universal-line range is introduced. By eliminating input bridge diodes, the proposed rectifier's efficiency is further improved. Moreover, the rectifier doubles its output voltage, which extends useable energy of the bulk capacitor after a dropout of the line voltage. The operation and performance of the proposed circuit was verified on a 700-W, universal-line experimental prototype operating at 65 kHz. The measured efficiencies at 50% load from 115 and 230 V line are both close to 96.4%. The efficiency difference between low line and high line is less than 0.5% at full load. A second-stage half-bridge converter was also included to show that the combined power stages easily meet Climate Saver Computing Initiative Gold Standard.

Index Terms—Bridgeless rectification, buck converter, power factor correction (PFC), voltage doubler.

I. INTRODUCTION

DRIVEN by economic reasons and environmental concerns, maintaining high efficiency across the entire load and input-voltage range of today's power supplies is in the forefront of performance requirements. Specifically, meeting and exceeding U.S. Environmental Protection Agency's (EPA) Energy Star [1], and Climate Saver Computing Initiative (CSCI) [2] efficiency specifications have become a standard requirement for both multiple- and single-output offline power supplies. Generally, the EPA and CSCI specifications define minimum efficiencies at 100%, 50%, and 20% of full load with a peak efficiency at 50% load. For example, for the highest performance tier of single-output power supplies with a 12-V output, i.e., for the Platinum level power supplies, the required minimum efficiencies at 100%, 50%, and 20% load, measured at 230 V line, are 92%, 94%, and 91%, respectively.

In universal-line (90–264 V) applications, maintaining a high efficiency across the entire line range poses a major challenge for ac/dc rectifiers that require power factor correction (PFC). For decades, a bridge diode rectifier followed by a boost converter has been the most commonly used PFC circuit because of its simplicity and good PF performance. However, a boost PFC front-end exhibits 1%–3% lower efficiency at 100 V line compared to that at 230 V line. This drop of efficiency at low line can be attributed to an increased input current that produces higher

losses in semiconductors and input electromagnetic interference filter components.

Another drawback of the universal-line boost PFC front-end is related to its relatively high output voltage, typically in the 380–400 V range. This high voltage not only has a detrimental effect on the switching losses of the boost converter, but also on the switching losses of the primary switches of the downstream dc/dc output stage and the size and efficiency of its isolation transformer. Because switching losses dominate at light loads, the light-load efficiency of a power supply exhibits a steep fall-off as the load current decreases.

At lower power levels, i.e., below 850 W, the drawbacks of the universal-line boost PFC front-end may partly be overcome by implementing the PFC front-end with a buck topology. As it has been demonstrated in [3], the universal-line buck PFC front-end with an output voltage in the 80 V range maintains a high-efficiency across the entire line range. In addition, a lower input voltage to the dc/dc output stage has beneficial effects on its light-load performance because lower voltage-rated semiconductor devices can be used for the dc/dc stage and because lower input voltage reduces the loss and size of the transformer.

The buck PFC converter operation in both discontinuous current mode and continuous current mode (CCM) was described first in [4], whereas additional analysis and circuit refinements were described in [5]–[12]. Because the buck PFC converter does not shape the line current around the zero crossings of the line voltage, i.e., during the time intervals when the line voltage is lower than the output voltage, it exhibits increased total harmonic distortion (THD) and a lower PF compared to its boost counterpart. As a result, in applications where IEC61000-3-2 and corresponding Japanese specifications (JIS-C-61000-3-2) need to be met, the buck converter PFC employment is limited to lower power levels.

In this paper, a bridgeless buck PFC rectifier that further improves the low-line (115 V) efficiency of the buck front-end by reducing the conduction loss through minimization of the number of simultaneously conducting semiconductor components is introduced. Because the proposed bridgeless buck rectifier also works as a voltage doubler, it can be designed to meet harmonic limit specifications with an output voltage that is twice that of a conventional buck PFC rectifier. As a result, the proposed rectifier also shows better hold-up time performance. Although the output voltage is doubled, the switching losses of the primary switches of the downstream dc/dc output stage are still significantly lower than that of the boost PFC counterpart.

It should be noted that a bridgeless voltage-doubler boost topology has been introduced in [13]. However, because this topology operates with the output voltage higher than twice the peak input voltage, i.e., with an output voltage of around 800 V, its employment in universal-line applications is not

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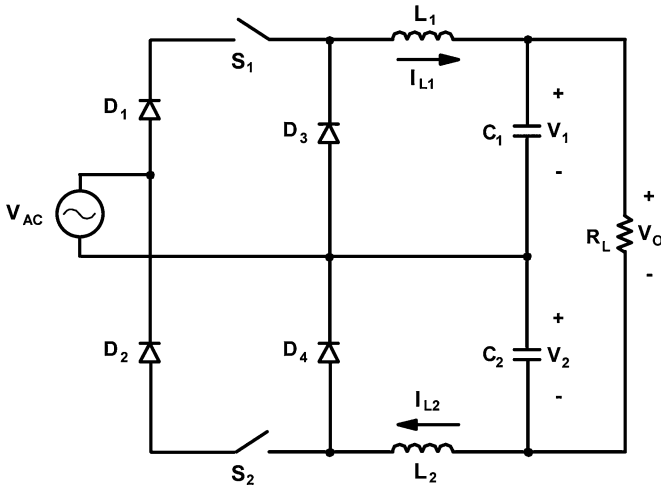


Fig. 1. Proposed bridgeless buck PFC rectifier.

practical with high-voltage semiconductor switches available today. Specifically, high-voltage silicon insulated gate bipolar transistors and MOSFETs with voltage ratings in the 1000–1200 V range that are required to implement this topology in universal-line applications exhibit increased losses and are more expensive than their counterparts rated at 600 V and below. In fact, the bridgeless voltage-doubler boost rectifier topology will become attractive from a performance point of view once high-voltage SiC and/or GaN devices become available in the future.

To verify the operation and performance of the proposed bridgeless buck PFC rectifier, a 700-W, universal-line experimental prototype operating at 65 kHz was built. The measured efficiencies at 50% load over the input voltage range from 115 to 230 V are more than 96%. In addition, the full-load efficiency difference between low line and high line is less than 0.5%. Including a half-bridge dc/dc converter 12-V output stage, the measured total efficiency is well above the CSCI Gold Level efficiency targets of 115 and 230 V line.

II. BRIDGELESS BUCK PFC RECTIFIER WITH VOLTAGE DOUBLER OUTPUT

The proposed PFC rectifier, as shown in Fig. 1, employs two back-to-back connected buck converters that operate in alternative halves of the line-voltage cycle. The buck converter illustrated in Fig. 2 only operates during positive half-cycles of line voltage V_{ac} and consists of a unidirectional switch implemented by diode D_1 in series with switch S_1 , freewheeling diode D_3 , filter inductor L_1 , and output capacitor C_1 . During its operation, the voltage across capacitor C_1 , which must be selected lower than the peak of line voltage, is regulated by pulse width modulation (PWM) of switch S_1 . Similarly, the buck converter consisting of the unidirectional switch implemented by diode D_2 in series with switch S_2 , freewheeling diode D_4 , filter inductor L_2 , and output capacitor C_2 operates only during negative half-cycles of line voltage V_{ac} , as shown in Fig. 3. During its operation, the voltage across capacitor C_2 is regulated by the PWM of switch S_2 .

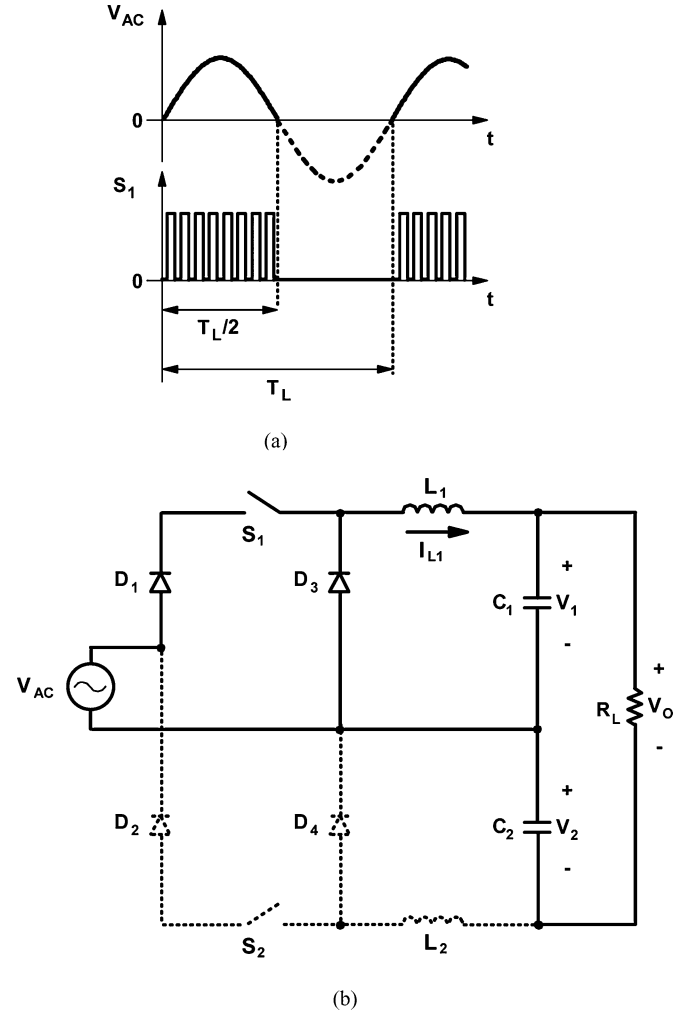


Fig. 2. Operation of the proposed bridgeless buck PFC rectifier during the period when the line voltage is positive.

As seen from Figs. 2 and 3, the input current always flows through only one diode during the conduction of a switch, i.e., either D_1 or D_2 . Efficiency is further improved by eliminating input bridge diodes in which two diodes carry the input current. An additional advantage of the proposed circuit is its inrush current control capability. Since the switches are located between the input and the output capacitors, switches S_1 and S_2 can actively control the input inrush current during start-up.

Output voltage V_{out} of the PFC rectifier, which is the sum of the voltages across output capacitors C_1 and C_2 , is given by

$$V_{out} = 2DV_{in} \quad (1)$$

where D is the duty cycle and V_{in} is the instantaneous rectified ac input voltage. Because of the buck topology, the relationship shown in (1) is valid for input voltages V_{in} greater than half the output voltage, i.e., for $V_{in} > V_{out}/2$. When input voltage V_{in} falls below $V_{out}/2$, the converters do not deliver energy from the input to the output so the load current is maintained solely by the output capacitors.

Because the PFC buck rectifier does not shape the line current during the time intervals when the line voltage is lower than

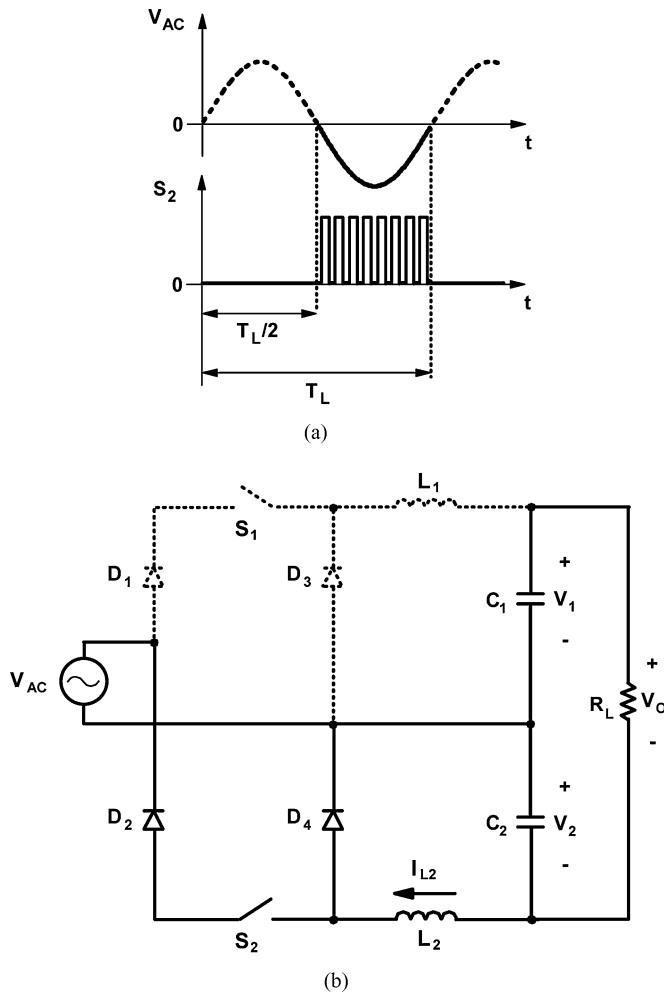


Fig. 3. Operation of the proposed bridgeless buck PFC rectifier during the period when the line voltage is negative.

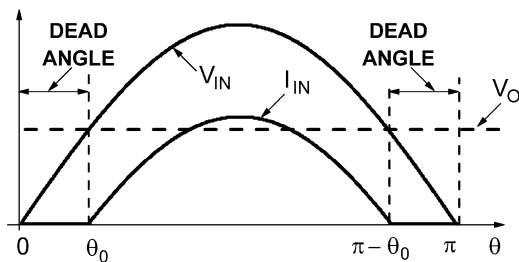


Fig. 4. Ideal input voltage and input current waveforms of a PFC buck rectifier.

the output voltage, as shown in Fig. 4, there is a strong trade-off between the THD and PF performance and output voltage selection. Namely, the output voltage should be maximized to minimize the size of the energy-storage capacitors for a given hold-up time. However, increasing the output voltage increases the THD and lowers the PF due to the increased dead angle, as shown in Fig. 4, i.e., the time the buck converter does not operate during a half-line cycle. It was found that for power levels below 850 W, output voltage should be kept below 160 V to meet the IEC61000-3-2 harmonic requirements. It should also be noted that the switching losses of the proposed rectifier is significantly

low, because the rectifier does not operate during the time when the input voltage is lower than half the output voltage.

As demonstrated in [3], clamped-current-mode control [14]–[16] is an effective, simple, and low-cost approach for controlling the buck PFC converter. Clamped-current-mode control can be easily extended to the bridgeless buck PFC front-end since during each half-cycle only one buck converter in the bridgeless PFC operates at a time to regulate the voltage across its corresponding output capacitor.

As known from the general peak-current-mode theory in [17] and [18], to ensure the stability of the current loop in the clamped-current-mode control circuit operating in CCM with a duty cycle over 50%, the slope of the compensation (external) ramp S_e should be at least 50% of the maximum down slope of the inductor current $S_{f,\max}$, i.e.,

$$S_e = k_S S_{f,\max}, \quad k_S \geq 0.5. \quad (2)$$

Furthermore, as described in [3], optimum design cannot be achieved with a single value for k_S , i.e., minimize THD of input current and attain a high PF in the entire universal-input range. In universal-line applications, optimal design can only be achieved by a variable k_S that is increasing with input voltage. As found in [3], the optimal range for k_S is between 1 and 2 for nominal low line (115 V) and between 3 and 5 for nominal high line (230 V).

It should also be noted that in the proposed bridgeless buck PFC rectifier, dc voltages across output capacitors C_1 and C_2 are automatically balanced. Namely, for a regulated output voltage V_{out} , i.e., for a constant sum of the capacitor voltages V_1 and V_2 in Fig. 1, any mismatching of capacitor voltages V_1 and V_2 will create differences in the input-current conduction angles during the positive and negative half of a line period, which will correct the mismatching of capacitor voltages. For example, if voltage V_1 becomes greater than V_2 for whatever reasons, the conduction angle of the line current during the positive half of line cycle will be smaller than that during the negative half. Because of the extended conduction angle, capacitor C_2 , which has a lower voltage, will be charged more during negative half periods than capacitor C_1 , which has a higher voltage and is charged during positive half periods. This process will go on until the average voltages across capacitors C_1 and C_2 are balanced.

Generally, the mismatching of the values of buck inductors L_1 and L_2 is the primary cause of differences in output capacitor voltages V_1 and V_2 since the proposed bridgeless buck PFC rectifier employs peak-current-mode control. However, the voltage imbalance caused by the mismatching of buck inductors L_1 and L_2 is significantly limited by the compensation ramp that is already employed in the peak-current-mode control circuit to achieve stability and minimum THD. The explanation of the effect of the compensation ramp slope on the mismatching of average output capacitor voltages V_1 and V_2 due to the mismatched inductors L_1 and L_2 is provided in the Appendix. The mismatching of values of output capacitors C_1 and C_2 in the proposed rectifier causes differences in the ripples of output capacitor voltages V_1 and V_2 . However, in applications that require a hold-up time, i.e., where the values of capacitors C_1 and C_2 are large so their ripples are small, the mismatching of output

capacitors C_1 and C_2 is a negligible factor contributing to the imbalance of output capacitor voltages V_1 and V_2 .

The magnitude of common-mode noise of the proposed rectifier is similar to that of the conventional boost PFC rectifier. As can be seen in Fig. 1, return of the input source and the midpoint of output capacitors C_1 and C_2 are directly connected. As a result, there is no high dv/dt between the input terminals and the output terminals, which makes the proposed rectifier operate with low common-mode noise.

Four topological variations of the proposed bridgeless buck PFC rectifier are shown in Fig. 5. As shown in Fig. 5(a), inductors L_1 and L_2 in the PFC rectifier in Fig. 1 can be replaced with a single inductor connected at the midpoint of capacitors C_1 and capacitor C_2 and the return of the input source. Since the topology employs only one buck inductor, magnetic component utilization is better. However, this circuit may generate high common-mode noise because the induced voltage across inductor L_1 in Fig. 5(a) introduces high dv/dt between the input terminals and the output terminals.

As shown in Fig. 5(b) without increasing common-mode noise, the number of magnetic components can also be reduced to a single component by coupling inductors L_1 and L_2 of the rectifier in Fig. 1. Because the winding of inductor L_1 and the winding of inductor L_2 use the same core, the utilization of the core increases. However, it may require a customized core with its large window area to accommodate both windings since most commercially available toroidal-type cores are optimized to accommodate a single winding.

Another topological variation can be obtained by moving switches S_1 and S_2 in the PFC rectifier in Fig. 1 to the ac side, as shown in Fig. 5(c). In this implementation, a bidirectional switch is formed by the serial connection of switches S_1 and S_2 with their antiparallel diodes D_{S1} and D_{S2} . The driving circuit for switches S_1 and S_2 is simple because the source terminal of each switch is connected together. Yet another variation of the proposed bridgeless buck PFC rectifier is in Fig. 5(d). In this circuit, the anodes of freewheeling diodes D_3 and D_4 are connected directly to the negative and positive output rails, respectively, instead of to the midpoint of the output capacitors, as shown in Fig. 1. It is interesting to note that the circuit in Fig. 5(d) exhibits a nonlinear gain characteristic given by

$$V_{out} = \frac{2D}{1 + (1 - D)^2} V_{in}. \quad (3)$$

According to (3), if duty cycle D is near unity, i.e., when input voltage V_{in} is close to half of output voltage V_{out} , the input-to-output gain is similar to that shown in (1). However, if duty cycle D is near zero, i.e., when input voltage V_{in} is much greater than output voltage V_{out} , the input-to-output gain becomes

$$V_{out} = DV_{in} \quad (4)$$

which is similar to the input-to-output gain of a conventional buck converter. Because capacitors C_1 and C_2 are simultaneously charged during the time when any of output diodes D_3 or D_4 is conducting, i.e., capacitors C_1 and C_2 are continuously charged during the whole line cycle, and the line-frequency voltage ripple across the capacitors is smaller than those of the

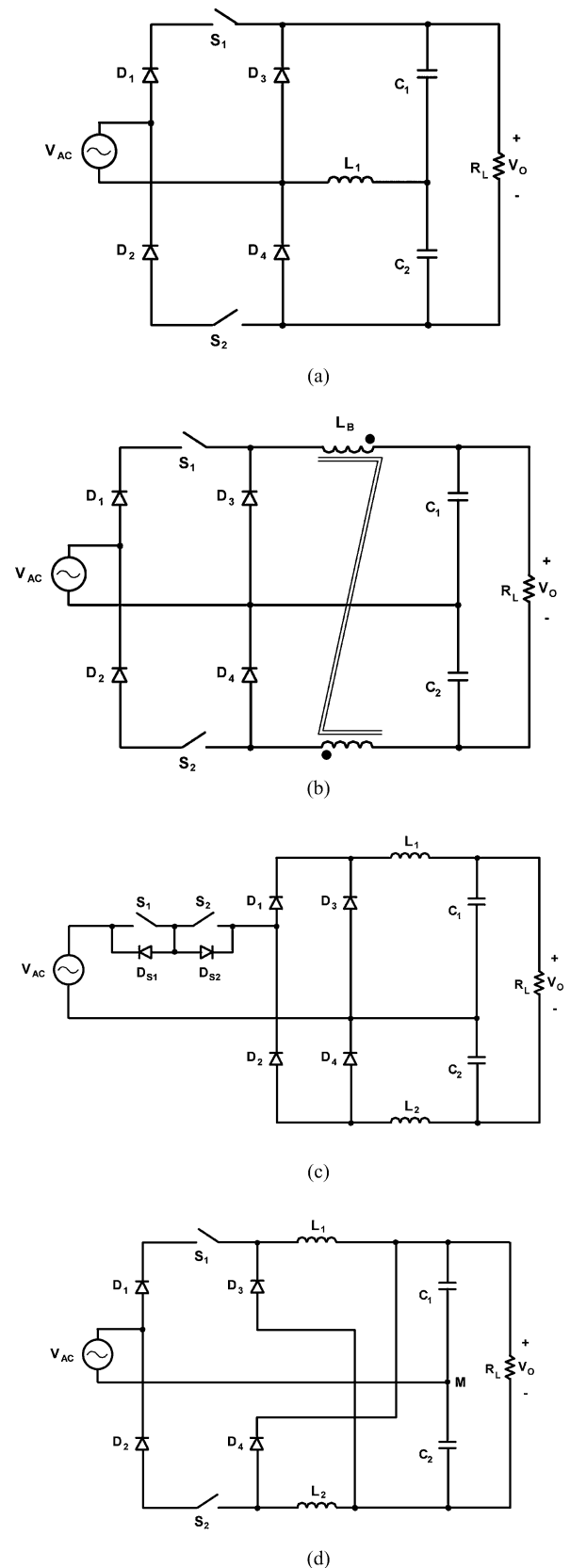


Fig. 5. Topology variations of the proposed bridgeless buck PFC rectifier. The rectifier with (a) single inductor, (b) coupled inductor, (c) bidirectional switch, and (d) nonlinear gain.

rectifier, as shown in Fig. 1. Finally, if reverse voltage blocking switches that allow unidirectional current flow are utilized for switches S_1 and S_2 , as shown in Figs. 1, 5(a), (b), and (d), diodes D_1 and D_2 can be eliminated.

III. EXPERIMENTAL RESULTS

The performance of the proposed rectifier in Fig. 1 was evaluated on a 65-kHz, 700-W prototype circuit that was designed to operate from a universal ac-line input (85–264 V_{RMS}) with a 160 V output. Fig. 6 shows the schematic diagram and component details of the experimental prototype circuit. Since the drain voltage of switches S_1 and S_2 are clamped to the voltage difference between the input voltage and output capacitor voltage, the peak voltage stress on switch S_1 and S_2 can be as high as 380 V, which is the peak input voltage at the maximum line. The peak current stress on switch S , which occurs at full load and low line, is approximately 9 A. Therefore, a STP42N65M5 MOSFET ($V_{DSS} = 650$ V, $R_{DS} = 0.079$ Ω) was used for each buck switch. Since buck diodes D_3 and D_4 must block both the same peak voltage stress and conduct the same peak current as the switches, an RHRP1560 diode ($V_{RRM} = 600$ V, $I_{FAVM} = 15$ A) was used.

It should be noted that in the universal-input bridgeless buck PFC rectifier there is no need to use SiC diode as in its boost counterpart since the reverse-recovery-related losses in the buck PFC are lower than those in the boost PFC. Because the reverse-recovery-related losses are given by the product of reverse-recovery charge Q_{RR} of the diode, the reverse voltage across the diode, and switching frequency f_s , these losses are lower in the buck PFC rectifier than in the boost because the reverse voltage across the diode is much smaller in the buck PFC rectifier. Whereas in the boost PFC the reverse voltage across the boost rectifier is equal to the output voltage, i.e., it is constant at 380–400 V, in the buck PFC the reverse voltage across the buck diode is given by the input voltage, which varies from zero to the peak of the line. At low line of 85 V_{RMS} , where the reverse-recovery losses are the greatest, the reverse voltage across the buck diode varies from 0 to $85 \times 1.414 = 120$ V, which is much smaller than that in its boost counterpart.

To obtain the desired inductance of output inductor L_1 and L_2 of approximately 60 μ H and also to achieve high efficiency at light load, the output inductor was built using a pair of ferrite cores (PQ-3225, DMR95) and 24 turns of Litz wire (0.1 mm, 110 strands). Litz wires were employed to reduce fringe effects near the gap area of the inductors [19]. Three aluminum capacitors (1000 μ F, 100 VDC) were used for output capacitors C_1 and C_2 for their ability to meet the hold-up time requirement (20 ms at 50% load and 12 ms at full load). Because capacitors C_1 and C_2 are connected in series, the capacitance seen from the second-stage converter is 1500 μ F. Although the total capacitance of capacitors C_1 and C_2 is 6000 μ F, the overall volume of the capacitors is not large since they are low-voltage capacitors.

As shown in Fig. 6, the bulk capacitor voltage that is the voltage across series connected capacitors C_1 and C_2 was regulated by a single controller (NCP1203). Switches S_1 and S_2 were operated simultaneously by the same gate signal from the

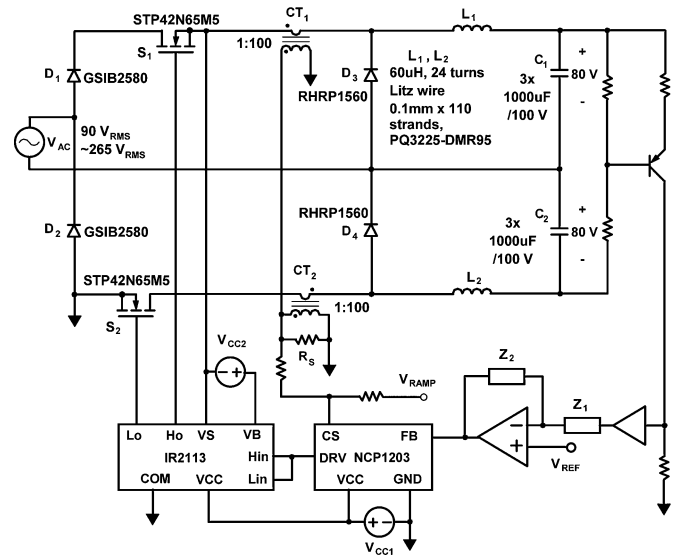


Fig. 6. Experimental prototype circuit of the proposed bridgeless buck PFC rectifier.

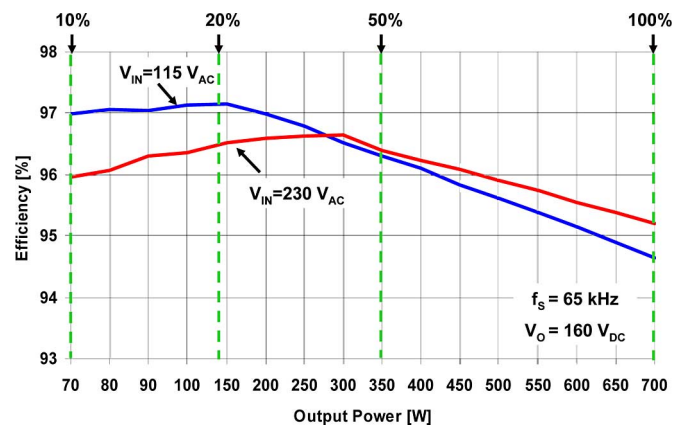


Fig. 7. Measured efficiency of the proposed bridgeless buck PFC rectifier.

PWM controller. Although both switches were always gated, only one switch carried positive current and delivered power to the output, i.e., switch S_1 on which the positive input voltage was induced, as shown in Fig. 2. The other switch on which the negative input voltage is induced, i.e., switch S_2 , as shown in Fig. 2, did not influence the operation since diode D_2 , which is connected in series with switch S_2 , blocked the current. It should be noted that the voltage across each capacitor C_1 or C_2 could also be independently regulated by two controllers. The independent controllers with a common output voltage reference actively balance the voltages across capacitors C_1 and C_2 so that the voltage imbalance by the mismatched output inductors can be completely eliminated.

Fig. 7 shows the measured efficiency of the proposed bridgeless buck PFC rectifier. It should be noted that the low-line efficiency is higher than the high-line efficiency over the load range below 40%. The efficiency difference between low line and high line is less than 0.5% over the load range above 50%, which is desirable for thermal optimization.

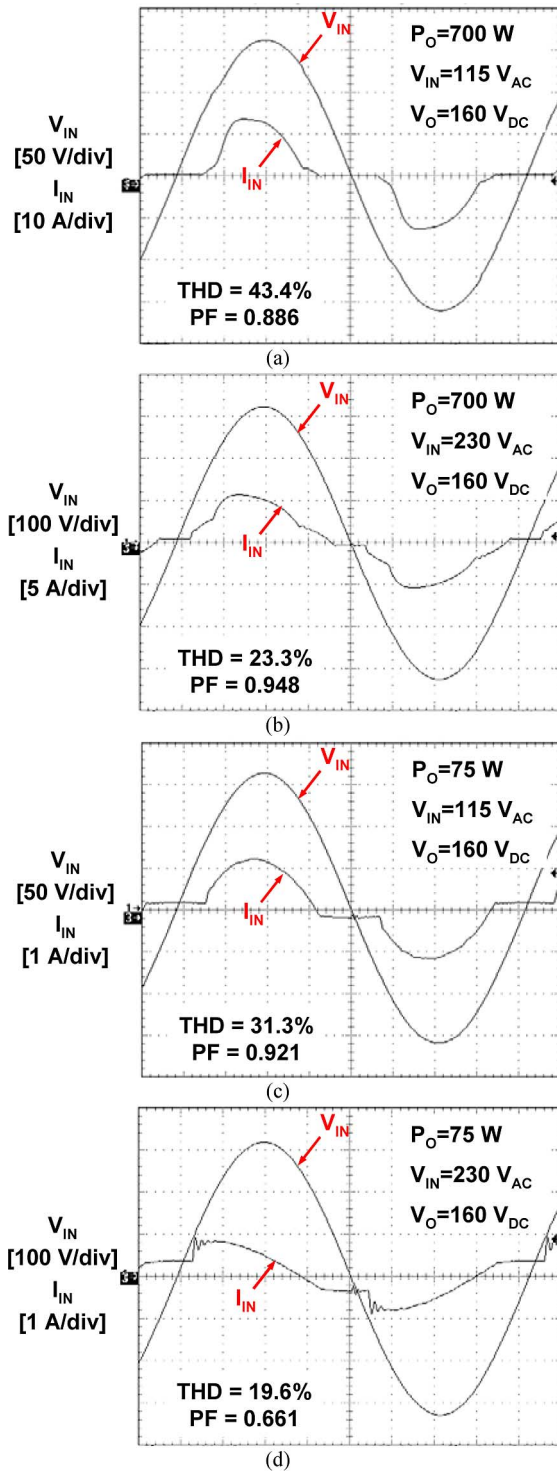


Fig. 8. Measured input voltage and current waveforms of the proposed bridgeless buck PFC rectifier when the output power is 700 W from (a) 115_{ac} and (b) 230_{ac} input voltage and 75 W from (c) 115_{ac} and (d) 230_{ac} input voltage.

Fig. 8 shows the measured input voltage and input current waveforms at 700- and 75-W for both low line (115_{ac}) and high line (230_{ac}). The measured THD and PF of the rectifier are also shown in the figures. Compliance of measured input-current harmonics at 700- and 75-W output power with Class D requirements of JIS C 6100-3-2 (measured at 115-_{ac} line

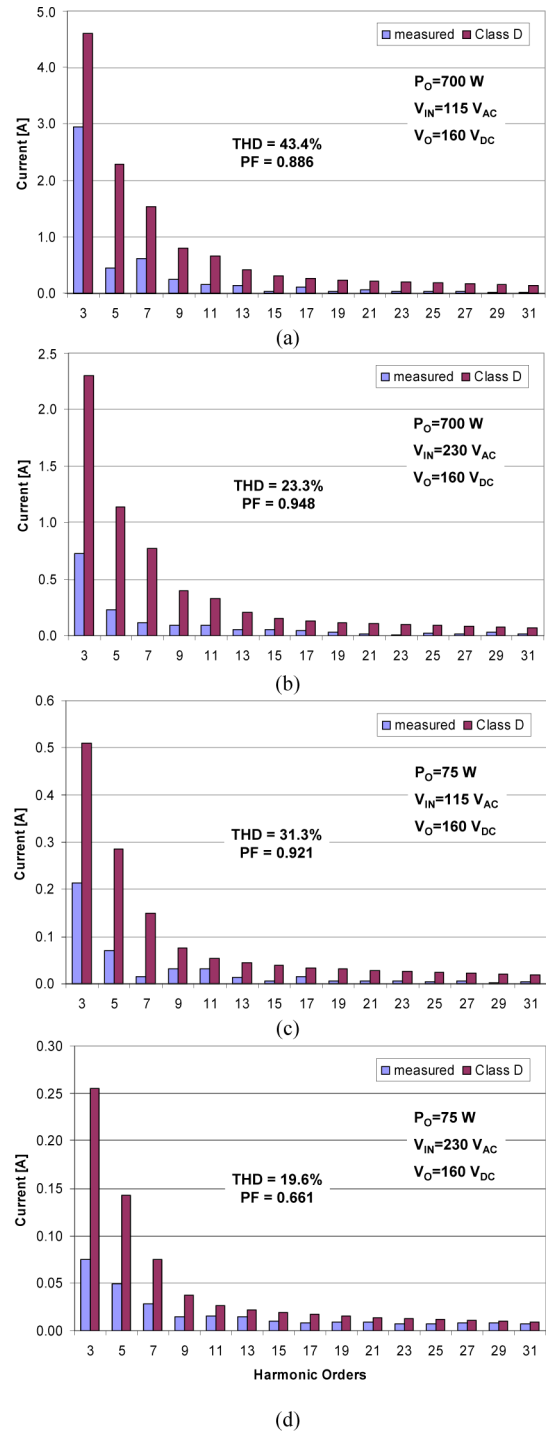


Fig. 9. Measured odd harmonic components of the input current at 700- and 75-W output power. Class D requirements of JIS C 6100-3-2 and IEC 61000-3-2 are also plotted.

voltage) and IEC 61000-3-2 (measured at 230-_{ac} line voltage) is given in Fig. 9. Because the input current is actively controlled by switch S_1 and S_2 of the proposed buck rectifier, the inrush current during start-up is well controlled, as shown in Fig. 10.

To verify the performance of the entire power supply using the proposed front-end rectifier, a conventional half-bridge

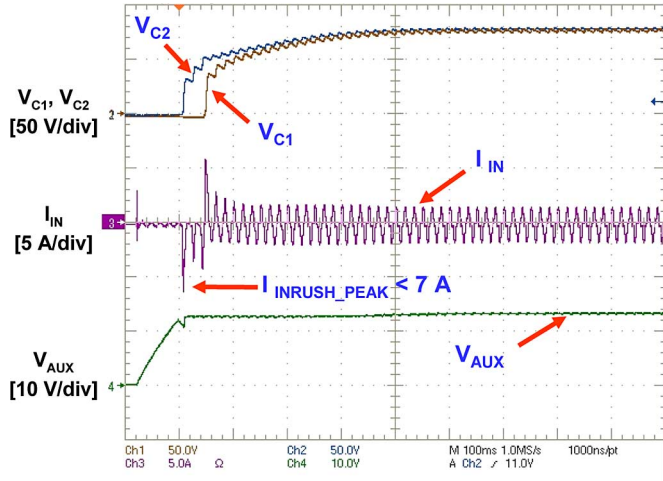


Fig. 10. Measured input current I_{in} , output capacitor voltages V_{C1} – V_{C2} and control voltage V_{AUX} of the experimental prototype circuit during start-up.

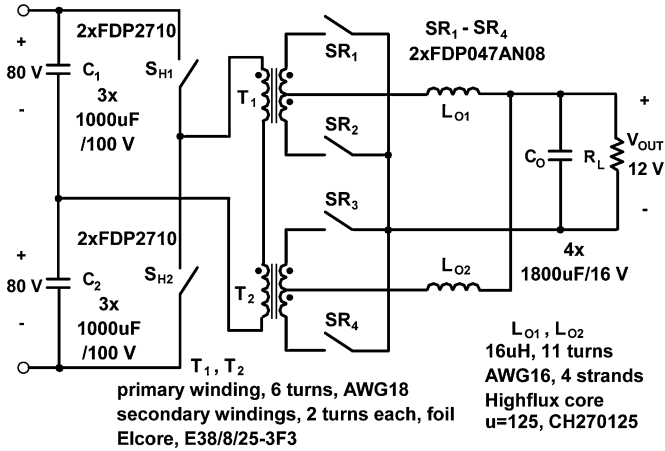


Fig. 11. Experimental half-bridge dc/dc second-stage converter. Input capacitors C_1 and C_2 are the same capacitors as the output capacitors of the front-end rectifier, as shown in Fig. 6.

converter with synchronous rectifiers was implemented as the second stage converter that operates at 65-kHz switching frequency and delivers 12- V_{dc} output voltage. Although any isolated dc/dc converter topology can be used for the second stage, a half-bridge dc/dc converter is a more suitable topology as the second stage converter for the proposed bridgeless buck PFC rectifier, because capacitors C_1 and C_2 , as shown in Fig. 6, are used as two bulk capacitors of the half-bridge converter.

Fig. 11 shows the experimental prototype circuit and the employed components. The second-stage half-bridge converter was implemented with two FDP2710 MOSFETs for each of bridge switches S_{H1} and S_{H2} and two parallel FDP047AN08AD MOSFETs for each of synchronous rectifier switches S_{R1} – S_{R4} . Transformer TR was built using a pair of ferrite cores (EI 38/8/25–3F3) with six turns of triple-insulated magnet wire (AWG #18) for the primary winding and two turns of copper foil for each of the secondary windings. Output filter inductors L_{O1} and L_{O2} were built using a toroidal high flux core (CH270125)

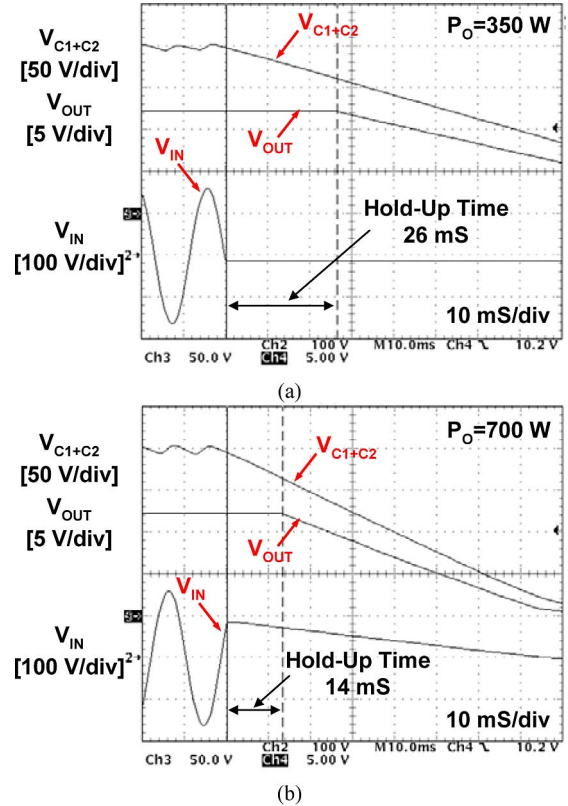


Fig. 12. Measured bulk capacitor voltage V_{C1+C2} that is the voltage across series connected capacitors C_1 and C_2 , output voltage V_{out} , and ac input voltage V_{in} at (a) 50% load and (b) 100% load during a hold-up time.

and 11 turns of magnet wire (4×AWG #16). Four low voltage aluminum capacitors (1800 μ F, 16 VDC) were used for output capacitor C_0 .

Fig. 12 shows the measured hold-up times at 50% load and full load conditions. Bulk capacitor voltage V_{C1+C2} , which is measured across the series-connected capacitors C_1 and C_2 of the front-end rectifier, and output voltage V_{out} of the dc/dc second-stage converter are shown in Fig. 12 together with input voltage V_{in} . The measured hold-up times are approximately 26 and 14 ms at 50% load and full load conditions, respectively.

The measured total efficiency of the proposed bridgeless buck PFC rectifier and half-bridge second-stage converter is plotted in Fig. 13. The power supply that delivers 12 V dc output from 115 and 230 V ac inputs meets the efficiency requirements of CSCI Gold specifications over the entire load and input ranges.

IV. SUMMARY

In this paper, a bridgeless buck PFC rectifier that substantially improves the efficiency at low line has been introduced. The proposed rectifier doubles the rectifier output voltage, which extends useable energy after a dropout of the line voltage. Moreover, by eliminating input bridge diodes, efficiency is further improved.

The operation and performance of the proposed circuit was verified on a 700-W, universal-line experimental prototype operating at 65 kHz. The measured efficiencies at 50% load from

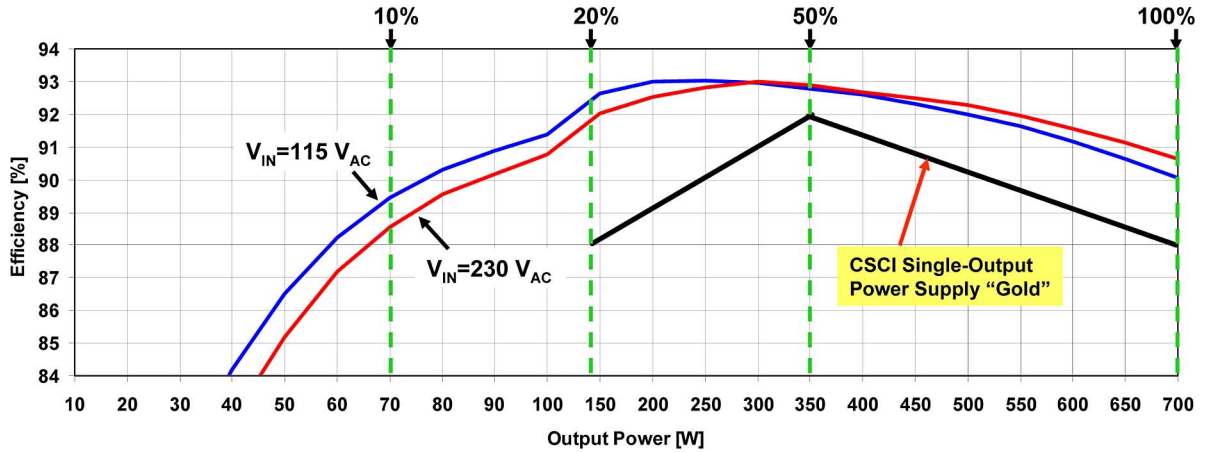


Fig. 13. Measured total efficiency of the proposed bridgeless buck PFC rectifier and half-bridge second-stage converter. The power supply delivers 12-V dc output from 115- and 230-V ac inputs. Efficiency requirements of CSCI “gold” specification are also plotted.

115 and 230 V line are close to 96.4%. The efficiency difference between low line and high line is less than 0.5% at full load. Finally, a half-bridge dc/dc converter is added as a second-stage converter. The measured total efficiency is well above the CSCI specifications at both 115 and 230 V line.

APPENDIX

EFFECT OF COMPENSATION RAMP SLOPE ON CAPACITOR VOLTAGE MISMATCHING DUE TO MISMATCHING OF FILTER INDUCTORS

To facilitate the explanation of the effect of the compensation ramp slope on the mismatching of average output capacitor voltages V_1 and V_2 , Fig. 14 shows the inductor current waveforms I_{L1} and I_{L2} for the case of mismatched inductances of inductors L_1 and L_2 ($L_1 < L_2$) and without compensation ramp. It should be noted that inductor currents I_{L1} and I_{L2} do not flow simultaneously, i.e., current I_{L1} flows during the positive half of the line cycle, whereas current I_{L2} flows during the negative half of the line cycle and, therefore, Fig. 14 shows inductor currents I_{L1} and I_{L2} at the same time instants in the corresponding line half cycles. As can be seen from Fig. 14, the mismatching of the inductors introduces mismatching in average inductor currents. Namely, because of a higher ripple, average current $\langle I_{L1} \rangle$ is smaller than average current $\langle I_{L2} \rangle$. This difference in the average inductor currents produces a difference in output capacitor voltages V_1 and V_2 .

Fig. 15 shows inductor current waveforms I_{L1} and I_{L2} when compensation ramp V_{RAMP} is added to the constant reference signal V_{REF} . As can be seen, with the addition of the ramp, the duty cycle of the buck converter having smaller filter inductor L_1 becomes smaller than the duty cycle of the buck converter with larger filter inductor L_2 . As a result, since the ripple of inductor current I_{L1} relative to that of inductor current I_{L2} is reduced with the addition of the ramp, the difference of inductor currents I_{L1} and I_{L2} in the presence of the ramp is smaller compared to that without the ramp. The smaller difference in the inductor currents produces a smaller difference in the output capacitor voltages V_1 and V_2 . In fact, slope of the ramp S_e can be found

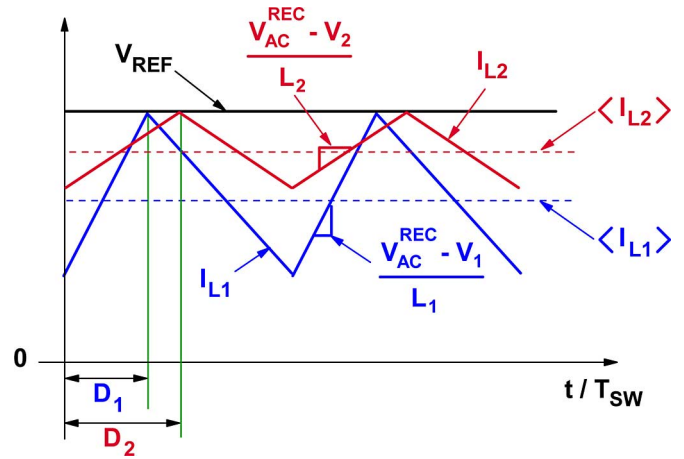


Fig. 14. Ideal inductor current waveform I_{L1} during the positive half-line cycle and ideal inductor current waveform I_{L2} during the following negative half-line cycle are plotted together with reference signal V_{REF} .

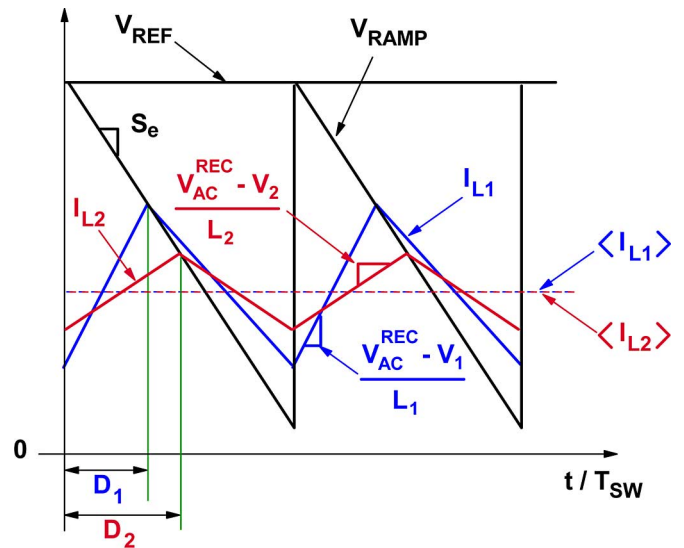


Fig. 15. Ideal inductor current waveform I_{L1} during the positive half-line cycle and ideal inductor current waveform I_{L2} during the following negative half-line cycle are plotted together with ramp signal V_{RAMP} and reference signal V_{REF} .

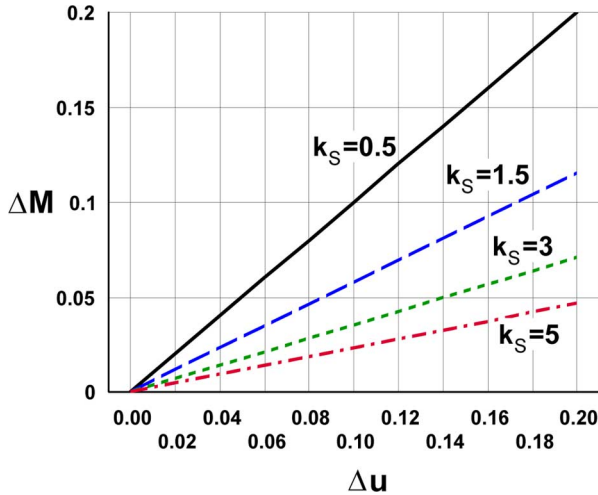


Fig. 16. Voltage difference ΔM between voltages V_1 and V_2 is plotted as function of inductance difference Δu between output inductors L_1 and L_2 .

for which average inductor currents are identical. In fact, this ideal situation is illustrated in Fig. 15.

Since capacitor voltages V_1 and V_2 are constant in steady-state operation, average current $\langle I_{L1} \rangle$ of inductor L_1 is equal to average current $\langle I_{L2} \rangle$ of inductor L_2 . As can be seen in Fig. 15, duty cycles D_1 and D_2 of switches S_1 and S_2 of the proposed rectifier are proportional to the positive slopes of inductor currents I_{L1} and I_{L2} , respectively. The voltage difference between capacitor voltages V_1 and V_2 and inductance difference between inductors L_1 and L_2 are related to duty cycles D_1 and D_2 , rectified input voltage V_{ac}^{REC} , and compensation ramp slope S_e , as shown in Fig. 15. Ramp slope S_e can be observed and described as

$$S_e = \frac{\frac{D_2}{2} \frac{(V_{ac}^{REC} - V_2)}{L_2} - \frac{D_1}{2} \frac{(V_{ac}^{REC} - V_1)}{L_1}}{D_2 - D_1}. \quad (A1)$$

The description of ramp slope S_e in (A1) can be simplified by using the expressions of voltage difference $M = V_1/V_2$ and inductance difference $U = L_1/L_2$. Voltage difference M also represents D_1/D_2 . The simplified expression of ramp slope S_e is

$$S_e = \frac{U (V_{ac}^{REC} - \frac{V_1}{M}) - M (V_{ac}^{REC} - V_1)}{2L_1 (1 - M)}. \quad (A2)$$

Moreover, by substituting voltage difference M and inductance difference U of (A2) for $1 + \Delta M$ and $1 + \Delta u$, respectively, and ignoring the second-order terms, ΔM is derived as

$$\Delta M = \frac{(V_{ac}^{REC} - V_1) \Delta u}{V_{ac}^{REC} - 2V_1 - 2S_e L_1}. \quad (A3)$$

Calculated values of ΔM as function of Δu in four cases of ramp slope S_e for the experimental circuit are plotted in Fig. 16. The four slopes of ramp signal S_e are labeled by values of k_S that is proportional to S_e , as shown in (2). The selected values of k_S are 0.5, 1.5, 3, and 5. It should be noted that the large slope of compensation ramp signal S_e significantly reduces voltage difference ΔM of the proposed rectifier when it

operates with the mismatched output inductors. It should also be noted that the imbalance of output voltage V_1 and V_2 , as shown in Fig. 16, as function of the mismatched inductors L_1 and L_2 is a calculated estimation without considering the effect of the automatic balancing by the input-current conduction angles due to the mismatching of capacitor voltages V_1 and V_2 described in Section II. In fact, the imbalance of output voltage V_1 and V_2 of the proposed rectifier with compensation ramp slope $k_S > 1.5$ and mismatched inductors L_1 and L_2 (10%) was practically unnoticeable during the experiment.

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