Performance Comparison of PI and P Compensation in DSP-Based Average-Current-Controlled Three-Phase Six-Switch Boost PFC Rectifier

Laszlo Huber, Misha Kumar, and Milan M. Jovanović

Abstract – In this paper, it is shown that in the three-phase six-switch boost PFC rectifier with average-current control with mismatched input-voltage and input-current sensing gains as well as offset errors in input-voltage and input-current sensing, the current controller with proportional (P) compensation exhibits lower total harmonic distortion (THD) and higher power factor (PF) compared with that of proportional and integral (PI) compensation. It is also shown that PI compensation with input-voltage feedforward is effective in improving output-voltage transient response with respect to input-voltage changes only if duty-cycle feedforward is also implemented. Finally, it is shown that zero-sequence-signal (ZSS) injection, in addition to enabling the output-voltage regulation in a wider input-voltage range, also improves the THD of the input currents.

Index Terms – Three-phase six-switch boost PFC rectifier, average-current control, PI compensation, voltage feedforward (VFF), duty-cycle feedforward (DFF), zero-sequence signal (ZSS) injection, mismatched sensing gains, offset errors, total harmonic distortion (THD), power factor (PF).

I. INTRODUCTION

Today, active three-phase PFC rectifiers need to meet very challenging performance requirements. In the majority of applications, the input current of active three-phase PFC rectifiers is required to have a total harmonic distortion (THD) less than 5% and a power factor (PF) greater than 0.99 [1]. One of the most cost-effective topologies that can meet these requirements is the three-phase six-switch boost PFC rectifier [2], which is usually implemented without neutral-point connection.

Many control methods that can achieve a high quality of input currents in the three-phase six-switch boost PFC rectifier are available [3], [4]. Generally, approaches using direct control of input current result in better quality of the input currents compared to those using direct power control [5]. Today, the control circuit is usually implemented with digital technology. One direct current control method, well suited for digital implementation, is average-current control [6], [7].

Fundamentally, the average-current control of the three-phase six-switch boost PFC rectifier supplied from a three-wire power system, i.e., without neutral-point connection, can be implemented with three independent current controllers with a common triangular carrier [5], [8]. It was shown in [5] that although the three-phase currents in such a system are not independent because of the neutral-point connection, the sum of the phase currents is zero, the whole rectifier system is stable if the equivalent single-phase control loops are stable. By adding appropriate zero-sequence-signals to the output of the current controllers, advanced control methods can be achieved which are equivalent to different continuous and discontinuous space vector modulation methods [9]-[12].

In the average-current control, the output-voltage controller is usually implemented with PI compensation to make the output voltage follow the output-voltage reference with minimum error, whereas, the current controller can be implemented with PI [13] or P compensation [5]. The average-current control in most implementations also includes voltage feedforward (VFF), zero-sequence-signal (ZSS) injection, and duty-cycle feedforward (DFF). With VFF, it can be achieved that the output voltage is practically insensitive to the line-voltage variations [6]. Generally, in boost PFC rectifiers, ZSS injection is employed to extend the input-voltage regulation range and/or to reduce the output voltage. With ZSS injection, the maximum input-voltage amplitude for a given output voltage can be increased by up to 15% [11]. Finally, DFF is mostly employed when current controllers with PI compensation are used to reduce the phase shift between a phase voltage and phase current and, consequently, improve the PF [14].

It should be noted that if the output-filter capacitance is very small, the low-frequency ripple in the output voltage can be considerable, resulting in increased distortions in the input currents. To reduce these distortions, the triangular carrier can be modulated with the output voltage waveform [15]. However, in applications where the output-filter capacitance is relatively large such as in applications that require hold-up time, which are primarily considered in this paper, the output-voltage ripple is generally very small and its effect on the input-current distortions is negligible.

Although design considerations for the current controllers in three-phase rectifiers are almost identical to those for single-phase rectifiers, the performance of the three-phase three-wire rectifiers under unbalanced conditions, caused by unbalanced input voltages, mismatched sensing gains, and offset errors in input-voltage and input-current sensing, can be significantly different from that of single-phase rectifiers due to the coupling of the input phase currents.

In this paper, it is shown that in the three-phase six-switch boost PFC rectifier with average-current control and mismatched input-voltage and input-current sensing gains as well as offset errors in input-voltage and input-current sensing, the current controller with P compensation exhibits better performance, i.e., lower THD and higher PF, compared with that of the PI compensation. It is also shown that the DFF, in addition to reducing the phase shift between the respective input voltages and currents in the PI-compensation implementation, significantly improves the effectiveness of VFF in the P-compensation implementation. Finally, it is
shown that ZSS injection improves the THD of input-currents in both current controllers with PI and P compensation. The operation with PI and P compensation is illustrated with Matlab/Simulink simulation waveforms and experimentally verified on a 3-kW prototype.

II. POWER STAGE AND CONTROL CIRCUIT

The simplified circuit diagram of the three-phase six-switch boost PFC rectifier used in this study is shown in Fig. 1. The evaluation circuit was designed with the following basic specifications:

- input phase-voltage range: 120 ± 15% Vrms
- line-frequency range: 45-65 Hz
- nominal output voltage: 400 V
- maximum output power: 3 kW

The switches are implemented with an IGBT six-pack module [16]. The switching frequency is selected as $f_{sw} = 20$ kHz, which is the maximum recommended $f_{sw}$ for the selected IGBT module. The values of boost inductors and output filter capacitors are $L_a = L_b = L_c = 1$ mH and $C_p = C_n = 2240$ µF, respectively.

The block diagram of the average-current control that is implemented with digital signal processor (DSP) TMS320F2808 from TI [17] is also shown in Fig. 1. For average-current control, the input phase-to-phase voltages, phase currents, and the output voltage are sensed. The input phase-to-phase voltages and the output voltage are sensed by using differential amplifiers, whereas, the phase currents are sensed by using Hall sensors and differential amplifiers. As shown in Fig. 1, the sensing gain of the input phase-to-phase voltages, phase currents, and output voltage are denoted as $K_v$, $K_i$, and $K_o$, respectively. The sensed voltages and currents are converted to digital signals through the 12-bit analog-digital converter (ADC) of the DSP. The input-voltage range of the ADC is 0-3 V, i.e., the full-scale range FSR = 3 V. Since only positive voltages can be applied to the input of the ADC, the bipolar phase-to-phase voltages and the bidirectional phase currents are scaled to ±FSR/2 and level shifted by FSR/2. The output signals of the DSP are the digital PWM (DPWM) gate signals for the bottom switches $S_{bn}$, $x \in \{a, b, c\}$. The gate signals for the upper switches are the complementary signals of the bottom switches. The DPWM is implemented with a triangular carrier, i.e., up-down counter. As the clock frequency of the DSP is $f_{sysclock} = 100$ MHz, the peak value of the triangular carrier (i.e., the maximum counter value) is $C_{pk} = f_{sysclock}/(2f_{sw}) = 2500$. All the sensed signals are sampled at the peak of the triangular carrier. The sampling frequency $f_s = f_{sw}$.

As shown in Fig. 1, the average-current control is implemented with VFF represented by the $K_{vAB/C^2}$ block [6]. The voltage controller is implemented with an adaptive PI compensation so that the voltage-loop bandwidth is 10 Hz in steady-state operation to meet the strict phase-current THD requirements and 100 Hz during load transients to reduce the output voltage overshoot and undershoot. The proper compensator is determined by monitoring the output-voltage error. Whenever the absolute error exceeds 2.1 V, the controller changes from the low-bandwidth to the high-bandwidth compensator. To avoid controller-output bouncing, the change from the high-bandwidth to the low-bandwidth compensator is implemented with a 1.5-V hysteresis, i.e., the change occurs when the absolute error falls below 0.6 V. The parameters of the adaptive digital PI compensator (z-domain parameters) are $\mathbf{K}_{pV,HBW} = 30.9$, $\mathbf{K}_{iV,HBW} = 29.2$ and $\mathbf{K}_{pV,LBW} = 10^{-3}$ and $\mathbf{K}_{pI,LBW} = 3.3 \cdot 10^{-3}$ and $\mathbf{K}_{pV,HBW} = 29.2 \cdot 10^{-3}$ for the 10-Hz and 100-Hz bandwidth, respectively. The current controller with PI and P compensation is designed so that the current-loop bandwidth is 2-kHz and 2.5-kHz, respectively, which both result in 45° phase margin. The PI compensation also includes a conditional anti-windup implementation [18]. The z-domain parameters of the PI and P compensator are $\mathbf{K}_{pl,PI} = 2640$, $\mathbf{K}_{il,PI} = 124$ and $\mathbf{K}_{pl,P} = 3337$, respectively. The design of the...
current and voltage controllers is outlined in Appendix A.

It is also shown in Fig. 1 that the control implementation includes ZSS injection and DFF. Injected ZSS value $v_{ZSS}^*$ is obtained as the negative average of the positive and negative envelopes of the input phase voltages (symmetrical ZSS) [11], i.e., as

$$v_{ZSS}^* = \frac{\text{max}(v_{a0}^*, v_{b0}^*, v_{c0}^*) - \text{min}(v_{a0}^*, v_{b0}^*, v_{c0}^*)}{2} = \frac{v_{ep}^* + v_{en}^*}{2}$$

(1)
The value of DFF signal $D_{FFx}^*$ for each phase is obtained directly from the corresponding phase voltage. It should be noted that without DFF, the ZSS signal can also be obtained from the output signals of the current controllers $D_{CCx}^*$. However, when DFF is employed, the duty cycle of the switches in steady-state operation is dominated by the DFF signals and, therefore, the ZSS injection obtained from the output signals of the current controllers is not effective. As shown in Fig. 1, the duty cycle of the bottom switches is obtained as

$$D_{oa}^* = \frac{1}{2} + D_{FFa}^* + D_{ZSS}^* + D_{CCa}^* = \frac{1}{2} + \frac{v_{a0}^* + v_{ZSS}^*}{v_{oef}} + D_{CCa}^* = \frac{1}{2} + \frac{v_{a0}^* + v_{ZSS}^*}{v_{oef}}$$

(2),

where output of current controller $D_{CCx}^*$ is much smaller than the DFF+ZSS term $D_{FFx}^* + D_{ZSS}^*$.

Finally, it should be noted that in order to meet the dead-time requirements for the IGBT module [16] and taking into

FIG. 2 Simulated waveforms of phase voltages and inductor currents in steady-state operation ($120\text{Vrms}, 2\text{kW}$) with PI compensation (with VFF, without ZSS injection and DFF), with offset errors in sensing: (a) phase voltages [V]; inductor currents [A], at (b) matched sensing gains, (c) mismatched current-sensing gains ($K_{csa}=0.9K_{csb}, K_{csb}=K_{csc}$), (d) mismatched voltage-sensing gains ($K_{vsab}=0.9K_{vsbc}, K_{vsbc}=K_{vsca}$).

FIG. 3 Simulated waveforms of phase voltages and inductor currents in steady-state operation ($120\text{Vrms}, 2\text{kW}$) with PI compensation (with VFF, without ZSS injection and DFF), with offset errors in sensing: (a) phase voltages [V]; inductor currents [A], at (b) matched sensing gains, (c) mismatched current-sensing gains ($K_{csa}=0.9K_{csb}, K_{csb}=K_{csc}$), (d) mismatched voltage-sensing gains ($K_{vsab}=0.9K_{vsbc}, K_{vsbc}=K_{vsca}$).

account the propagation delay times of the optocouplers in the interface circuit between the DSP and IGBT module [19], the duty-cycle range is limited from $D_{min,Lim}=0.07$ to $D_{max,Lim}=0.93$.

III. PERFORMANCE COMPARISON OF CURRENT CONTROLLERS WITH PI AND P COMPENSATION

A. Steady-State Operation

First, steady-state performance comparison of current controllers with PI and P compensation implemented only with VFF, i.e., without ZSS injection and DFF, is done. The comparison is performed for balanced input voltages for both matched and mismatched sensing gains, and without offset errors in input-voltage and input-current sensing. As an example, simulated waveforms of phase voltages and inductor currents at nominal phase voltage of 120 Vrms and 2-kW load with PI and P compensation are presented in Figs. 2 and 3, respectively. The inductor-current waveforms in Figs. 2(b) and 3(b) are obtained with matched sensing gains ($K_{vsab}=K_{vsbc}=K_{vsca}$ and $K_{csa}=K_{csb}=K_{csc}$), in Figs. 2(c) and 3(c) with mismatched current-sensing gains ($K_{csa}=0.9K_{csb}, K_{csb}=K_{csc}$), and in Figs. 2(d) and 3(d) with mismatched voltage-sensing gains ($K_{vsab}=0.9K_{vsbc}, K_{vsbc}=K_{vsca}$).

With matched sensing gains, the waveform of the inductor currents with both PI and P compensation is almost perfectly sinusoidal with THDs slightly greater than 2%. However, as shown in Fig. 2, the inductor currents with PI compensation are significantly phase shifted with respect to the phase voltages ($\phi \sim -16.5\degree$), which results in a reduced PF. To explain

THDc=8.07% THDa=2.02% THDb=2.01% THDc=2.05% THDa=1.96% THDb=2.06% THDc=4.68% THDa=3.64% THDb=3.46% THDc=2.11% THDa=2.08% THDb=2.08% THDc=2.08% THDa=2.08% THDb=2.08%
the origin of the phase shift, Fig. 4 shows the input and output waveforms of the PI current controller. To achieve a sinusoidal current in phase x, where \( x \in \{a, b, c\} \), controller output \( D_{CCx} \) must be sinusoidal (and proportional to the negative value of the phase voltage), as shown in Fig. 4(d). Since the integrator introduces a phase shift of 90°, to obtain a sinusoidal signal at the output of the PI controller, the input of the controller \( i_{x,ERR} = i_{x,ref} - i_x \) must be a cosine signal, as illustrated in Fig. 4(c). This cosine signal at the input of the controller can only be generated as a difference of two phase-shifted sine signals, i.e., if there is a phase shift between sinusoidal signal \( i_{x,ref} \) that is proportional to the phase voltage and sinusoidal signal \( i_x \) that is proportional to the phase current, as shown in Fig. 4(b). It should be noted that the phase shift is proportional to the amplitude of the required input signal \( i_{x,ERR} \), which for a given PI-controller gain at line frequency is proportional to the amplitude of the output signal \( D_{CCx} \). Since when DFF is employed the output of the current controller \( D_{CCx} \) is very much reduced (because it only needs to correct for relatively small imperfections of DFF), the phase shift with DFF is also dramatically reduced.

With mismatched current-sensing gains, the quality of the inductor currents with P compensation, Fig. 3(c), is almost the same as that with perfectly matched sensing gains, Fig. 3(b). However, with mismatched current-sensing gains, the quality of the inductor currents with PI compensation, Fig. 2(c), is noticeably deteriorated compared to that with matched sensing gains, Fig. 2(b). This behavior can be explained by considering the output signal of the current controllers and the duty-cycle limits.

In steady-state operation, with matched sensing gains, without ZSS injection and DFF, the output signal of the current controllers is sinusoidal with amplitude

\[
D_{CCx,\text{max}}^* = \frac{V_m}{V_o} C_{pk}, \quad x \in \{a,b,c\}, \tag{3}
\]

where, \( V_m \) is the amplitude of the input phase voltages and \( V_o \) is the output voltage. It should be noted in (3) that \( D_{CCx,\text{max}}^* \) is scaled to peak value \( C_{pk} \) of the triangular carrier. At the nominal phase voltage of 120 Vrms,

\[
D_{CCx,\text{max}}^* = \frac{\sqrt{2} 120}{400} \cdot 2500 = 1061. \tag{4}
\]

Considering the duty-cycle limits, the linear-operation range is determined as

\[
D_{CCx,\text{lim}} = \frac{D_{\text{min},\text{lim}} - D_{\text{min},\text{lim}}}{2} \cdot 2500 = 0.93 - 0.07 = 2500 = 1075. \tag{5}
\]

From (4) and (5), it can be concluded that in this design the margin to compensate errors, such as dc offsets, mismatched sensing gains, and offset errors in input-voltage and input-current sensing, is very narrow, i.e.,

\[
\delta D_{CCx}^* < \frac{1075 - 1061}{1061} = 1.32\%. \tag{6}
\]

This narrow margin for compensation of errors has a detrimental effect on the current controllers with PI compensation. The simulations show that the output signal of the current controllers with PI compensation contains a negative dc offset such that even with matched sensing gains the minimum duty cycle is very close to the minimum limit. This dc offset is generated by the integrator and it is due to the non-zero steady-state error of the PI controller. In fact, when the reference signals are sinusoidal, the PI controller cannot achieve zero steady-state error due to the finite gain at the line frequency [20]. With mismatched current-sensing gains, the minimum duty cycle in phases “b” and “c”, which have larger current-sensing gain than phase “a”, becomes saturated, resulting in distorted phase currents as shown in Fig. 2(c). The effect of the duty cycle limits on the linear operation range of the current controller with PI compensation is illustrated in Fig. 5(a).

With mismatched voltage sensing gains, for both PI and P compensation, the quality of inductor currents is similar to that with mismatched current sensing gains, as shown in Figs. 2(c),(d) and 3(c),(d), respectively. Referring to Fig. 1, this similarity can be explained by recognizing that the mismatching of the current sensing gains produces differences at the negative input of the current controllers, i.e., differences in \( i_x \), whereas the mismatching of the voltage sensing gains produces differences at the positive input, i.e., differences in \( i_{x,ref} \). Since the input of the current controllers is \( i_{x,ERR} = i_{x,ref} - i_x \), the effect of the mismatching of the current and voltage gains at the input of the controller is the same. However, as shown in Figs. 2(c), (d) for the implementation with PI compensation, the THD of inductor currents with mismatched voltage sensing gains is slightly lower than that with the same mismatching of the current sensing gains. This is due to the fact that a 10% mismatch in phase-to-phase voltage sensing.
gains results in only 5% mismatch in calculated phase-to-neutral voltages which are used in determining $i_{ref}$.

Generally, for a given input voltage, the duty-cycle saturation margin can be increased by selecting a higher output voltage and/or extending the available duty-cycle range. Both approaches increase the difference between the required maximum (minimum) duty cycle and the duty-cycle limits. However, both approaches also suffer from major drawbacks that make them impractical in any applications. Besides increasing the size and cost of the output filter, increasing the output voltage of the three-phase front end beyond 420-450 V prevents the use of downstream dc-dc converters for single-phase applications that are typically designed for 340-420-V range. Widening the duty-cycle limits requires lowering the switching frequency and/or selecting faster switches and faster interface circuits, if available. Lowering the switching frequency below 20 kHz is not desirable because of increased size of magnetic components and possible audio-noise issues.

It should be noted that instead of PI controller, a proportional plus resonant (PR) controller can be employed, which results in zero steady-state error due to the infinite gain at resonant frequency, when the resonant frequency is set to the line frequency [4], [20]-[24]. It should be also noted that zero steady-state error can also be achieved with PI controller if the control is implemented instead of in the stationary (a,b,c) reference frame in the rotating (d,q) reference frame, where the sinusoidal signals are transformed to dc signals [3], [4], [20]-[25].

The power factor of the inductor currents with PI compensation can be vastly improved by implementing DFF. As shown in Fig. 6(b), with DFF, the phase shift of the phase currents with respect to the phase voltages is $\phi \sim 1.5^\circ$, which is a significant reduction compared to $\phi \sim 16.5^\circ$ without DFF in Fig. 2(b). As already explained, this phase-shift reduction is the result of the fact that with DFF the duty cycle of the switches in steady-state operation is dominated by the DFF signals, which are proportional to the phase voltages, while the effect of the output signals of the current controllers on the duty cycles is practically negligible. However, it should be also noted that with DFF, the distortion of the inductor currents with PI compensation and with mismatched current-sensing gains is approximately the same as that without DFF, as it can be seen in Figs. 2(c) and 6(c).

The THD of the inductor currents with PI compensation and with mismatched sensing gains can be improved by implementing ZSS injection, as illustrated in Fig. 7(c). In fact, with symmetrical ZSS injection, which is implemented in this paper, the effective amplitude of the input phase voltages is reduced to 86.6% $\sin(60^\circ)$, as shown Fig. 5(b). As a result, the maximum duty cycle is proportionally reduced,

$$D_{CCx,max} = \sqrt{2} \cdot 120 \cdot 0.866 \cdot \frac{400}{2500} = 918 \text{,}$$

and, therefore, more margin is available for compensation of errors, i.e.,

$$\Delta D_{CCx} < \frac{1075 - 918}{918} = 17.1\% \text{.}$$

This increased margin is sufficient to keep the duty cycle of the switches away from saturation at nominal phase voltage of 120 Vrms, as illustrated in Fig. 7(b). However, at maximum phase voltage of 138 Vrms, even with ZSS injection, the inductor currents are distorted with mismatched sensing gains, as shown in Fig. 8(c).

It should be noted in Fig. 7(b) that with ZSS injection, the THD of the inductor currents with PI compensation and matched sensing gains is also improved compared to that without ZSS injection shown in Fig 6(b). Specifically, the THD of the inductor currents is reduced from $\sim 2.1\%$ to $\sim 1.6\%$.

ZSS injection also improves the THD of inductor currents with P compensation, as shown in Fig. 9. Specifically, at 120-Vrms phase voltage and matched sensing gains, the THD of the inductor currents with P compensation and with ZSS injection is reduced to $\sim 1.7\%$ from $\sim 2.1\%$ without ZSS injection. This is the result of the reduced peak-to-peak ripple in the inductor currents at the peak values of the phase voltages, as it can be observed by comparing Figs. 9(b) and 9(c). In fact, it can be seen in Fig. 9 that the peak-to-peak ripple in the inductor current waveforms increases and decreases four times in a line cycle, having maximum values at the positive peak, negative peak, and zero-crossings of the input phase voltages. This means that the ripple current of inductors contains low-frequency (120 Hz and 240 Hz) harmonics, which contribute to the THD of the inductor currents. Since with ZSS injection the peak-to-peak ripple in the inductor currents decreases at the peaks of the input phase voltages compared to that without ZSS injection, the low-frequency ripple components of the inductor currents decrease, and, consequently, the THD decreases. An analysis of the peak-to-peak ripple in the inductor currents with and without ZSS injection is given in the Appendix B.

Finally, steady-state performance comparison of current controllers with PI and P compensation implemented with VFF, DFF, and with/without ZSS injection is done with offset errors in the input-current sensing (with matched sensing gains). As an example, with an equal offset error of 1.25% of FSR ($\Delta i_{offset} = -50(Q12)$) in all three input-current sensing circuits (same 1.5-V offset applied in all three phases, as shown in Fig. 1), simulated waveforms of phase voltages and inductor currents at nominal phase voltage of 120 Vrms and 2-kW load with PI and P compensation are presented in Figs. 10.
and 11, respectively. The inductor-current waveforms in Figs. 10(b) and 11(b) are obtained without ZSS injection and in Figs. 10(c) and 11(c) with ZSS injection. As shown in Fig. 11(b), with P compensation, the inductor currents with offset errors in the current sensing are only slightly distorted compared to those without offset errors in Fig. 9(b). However, as shown in Fig. 10(b), with PI compensation, the quality of inductor currents with offset errors in the current sensing is significantly deteriorated (THD_{a,b,c} \approx 13\%) compared to those without offset errors in Fig. 6(b). ZSS injection, as shown in Figs. 10(c) and 11(c), slightly improves the quality of inductor currents for both PI and P compensation. However, even with ZSS injection, the inductor currents with PI compensation are considerably distorted (THD_{a,b,c} \approx 9\%). This distortion in the inductor currents with PI compensation is caused by the integration error. It should be noted that identical offset errors in input-voltage sensing do not affect the quality of the input currents because an offset error in the phase-to-phase voltage sensing is cancelled in the calculated phase voltages because they are given by difference of phase-to-phase voltages. The THDs of inductor currents with PI and P compensation in steady-state operation at nominal phase voltage of 120 Vrms and 2-kW load at different operating conditions are summarized in Tables I and II, respectively. It can be
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concluded from Tables I and II that with mismatched sensing gains, no offset errors, and without ZSS injection, the THD of inductor currents with PI compensation is significantly higher than that with P compensation; whereas, with ZSS injection, the THD of inductor currents with PI compensation is similar to that with P compensation. However, in the whole input voltage range, PI compensation does not perform as well as P compensation. In fact, at the maximum phase voltage of 138 Vrms, even with ZSS injection, with mismatched sensing gains the inductor currents with PI compensation are distorted, as shown in Fig. 8(c). Finally, it can be concluded from Tables I and II that with offset errors and matched sensing gains, the THD of inductor currents with PI compensation, even with ZSS injection, is much higher than that with P compensation.

B. Operation with Phase-Voltage Transients

First, performance comparison of current controllers with PI and P compensation during phase-voltage transients is performed with balanced input voltages, matched sensing gains, no offset errors in input-current sensing, and for a control implemented with VFF and ZSS injection and without DFF. In this evaluation, the phase voltage is stepped from 102 Vrms to 138 Vrms and back to 102 Vrms at 2-kW load. It should be noted that ZSS injection was necessary to achieve output-voltage regulation in the entire input-voltage range from 102 Vrms to 138 Vrms. During the phase-voltage transients, the voltage-loop bandwidth was 10 Hz. Key simulated waveforms with PI and P compensation are presented in Figs. 12 and 13, respectively. It can be seen in Fig. 12 that the output voltage with PI compensation and VFF is almost insensitive to input voltage transients. The output voltage overshoots and undershoots when the amplitude of the input phase voltages step changes between 144 V and 195 V is around 3-4 V. However, as shown in Fig. 13, despite the VFF, the output voltage with P compensation exhibits a significant overshoot and undershoot (~20V) when the amplitude of the input phase voltages steps up from 144 V to 195 V and steps down from 195 V to 144 V, respectively. As can be seen from the waveforms in Figs. 12 (b) and (c), in the implementation with PI compensation the sensed inductor currents follow the reference currents, whereas in the implementation with P compensation the sensed inductor currents are very different from the reference currents, as shown in waveforms in Figs. 13 (b) and (c). This behavior of the P compensation can be explained by analyzing the output signal of the current controllers. For simplicity, the ZSS injection is not included in the following considerations.

In steady-state operation, without DFF and ZSS injection, the current controllers generate the desired duty cycles. Using the notations in Fig. 1, the following relationship can be written at the peak value of the phase voltage,

\[
K_p \cdot \left[ K_m \frac{V_m^*}{V_{FSR}} - \frac{K_{cs} V_m^*}{FSR \sqrt{2}} \cdot K_{FF}^2 \right] = \frac{V_m}{V_o} \cdot C_{pk}, \tag{9}
\]

where, the first and second term in the bracket represent the reference current and sensed current at the input of the current controller, respectively, \(K_p\) is the gain of the P compensation, \(I_m\) is the amplitude of the input phase currents, and \(K_{FF}\) is the conversion factor from rms to average value, i.e.,

\[
K_{FF} = \frac{2}{\sqrt{2}} = 0.9. \tag{10}
\]

The amplitude of the phase currents \(I_m\) can be expressed through the input-output power balance as
TABLE I – THD OF INDUCTOR CURRENTS WITH PI COMPENSATION (120Vrms, 2kW)

<table>
<thead>
<tr>
<th>Phase current sensing*</th>
<th>Phase-Phase voltage sensing*</th>
<th>PI w/o DFF, w/o ZSS</th>
<th>PI w/ DFF, w/o ZSS</th>
<th>PI w/ DFF, w/ ZSS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$K_{sa}$/$K_{cs}$</td>
<td>$K_{sb}$/$K_{cs}$</td>
<td>$K_{sc}$/$K_{cs}$</td>
<td>$\Delta I_{offset}$ [%FSR]</td>
<td>$K_{sa}$/$K_{cv}$</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0.9</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0.9</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0.9</td>
</tr>
<tr>
<td>0.9</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0.9</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1.25</td>
<td>1</td>
</tr>
</tbody>
</table>

* Sensing gains normalized to their matched values

TABLE II – THD OF INDUCTOR CURRENTS WITH P COMPENSATION (120Vrms, 2kW)

<table>
<thead>
<tr>
<th>Phase current sensing*</th>
<th>Phase-Phase voltage sensing*</th>
<th>P w/o DFF, w/o ZSS</th>
<th>P w/ DFF, w/o ZSS</th>
<th>P w/ DFF, w/ ZSS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$K_{sa}$/$K_{cs}$</td>
<td>$K_{sb}$/$K_{cs}$</td>
<td>$K_{sc}$/$K_{cs}$</td>
<td>$\Delta I_{offset}$ [%FSR]</td>
<td>$K_{sa}$/$K_{cv}$</td>
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<td>1</td>
<td>1</td>
<td>1.25</td>
<td>1</td>
</tr>
</tbody>
</table>

* Sensing gains normalized to their matched values

The effect of the DFF on phase-voltage transients with P compensation is presented in Fig. 14. It can be seen in Fig. 14 that the output voltage with P compensation when VFF is used along with DFF becomes practically insensitive to input-voltage transients. It should be noted that with DFF, the sensed inductor currents with P compensation properly follow the reference currents, as seen comparing waveforms in Figs. 14 (b) and (e). This behavior of the P compensation can be explained by considering how the switch duty cycles are generated. As already explained, in steady-state operation with DFF, the switch duty cycles are dominated by the DFF signals, whereas, the effect of the output signals of the current controllers on the duty cycles can be neglected, i.e., the output signals of the current controllers can be considered as zero. By equating the left-hand side of (9), which represents the output
of the current controllers, with zero, and by using (11), it is obtained that

$$V_{E_A} = \frac{K_{pb} K_{cs} K_{FF}^2}{3K_m FSR^2} P_o. \quad (13)$$

From (13), it can be seen that the voltage-controller output is independent of the peak value of the phase voltages. In fact, when the amplitude of the input phase voltages step changes between 144 V to 195 V, the voltage controller output $V_{E_A}$ changes only by approximately ±10 around 2240 (in Q12 format) to compensate the small changes in the output voltage due to the fact that the inductor currents cannot instantly change.

In the case of the PI compensation, when VFF is used with DFF, the output voltage overshoot and undershoot is practically negligible (less than 1 V) when the amplitude of the input phase voltages step changes between 144 V to 195 V.

IV. EXPERIMENTAL RESULTS

Experimental waveforms of phase voltage $v_{ab}$ and phase currents $i_a$, $i_b$, and $i_c$ in steady-state operation, at nominal phase voltage of 120 Vrms and 2-kW load, at balanced input voltages are presented in Figs. 15-20. It should be noted that the input-voltage and input-current sensing gains are not completely matched and that the offset in input-voltage and input-current sensing is not exactly 1.5-V due to component tolerances. The waveforms in Figs. 15 and 16 are obtained with PI and P compensation, respectively, for operation with VFF and ZSS injection, and without DFF. The waveforms in Figs. 17 and 18 are obtained with PI and P compensation, respectively, for operation with VFF and DFF, and without ZSS injection. Finally, the waveforms in Figs. 19 and 20 are obtained with PI and P compensation, respectively, for operation with VFF, DFF, and ZSS injection. Generally, these results are in good agreement with the simulated waveforms and verify that the current controller with PI compensation is more sensitive to mismatches in input-voltage and input-current sensing gains and offset errors in input-current sensing than the current controller with P compensation. It should be noted by comparing the measured phase currents with PI compensation in Figs. 17 and 19 with the corresponding simulated phase currents in Figs. 10(b) and 10(c) that the distortions in the measured phase currents are mainly caused by the offset errors in input-current sensing.

Finally, comparing the measured currents and PFs with PI compensation in Figs. 15, 17 and 19, it can be seen that DFF improves the PF with PI compensation from 0.956-0.959 to 0.998. The THD measurements with PI compensation in Figs. 15 and 19 compared to Fig. 17, and THD measurements with P compensation in Figs. 16 and 20 compared to Fig. 18 show that ZSS injection improves the quality of the input currents in both implementations.

V. CONCLUSION

In this paper, it is shown that in the three-phase six-switch boost PFC rectifier with average-current control and mismatched input-voltage and input-current sensing gains as well as offset errors in input-voltage and input-current sensing, the current controller with P compensation exhibits better performance, i.e., lower THD and higher PF, compared with that of the PI compensation. The sensitivity of the current controller with PI compensation to both mismatches in the sensing gains and offset errors in the input-current sensing is the result of the relatively small margin in the linear operation range (due to the limits of the switch duty cycles), which is
Fig. 15 Steady-state experimental waveforms (120Vrms, 2kW) with PI compensation (with VFF and ZSS injection, without DFF): (a) phase-voltage $V_{a0}$, (b) phase currents $I_a$, $I_b$, $I_c$.

Fig. 16 Steady-state experimental waveforms (120Vrms, 2kW) with PI compensation (with VFF and ZSS injection, without DFF): (a) phase-voltage $V_{a0}$, (b) phase currents $I_a$, $I_b$, $I_c$.

Fig. 17 Steady-state experimental waveforms (120Vrms, 2kW) with PI compensation (with VFF and DFF, without ZSS injection): (a) phase-voltage $V_{a0}$, (b) phase currents $I_a$, $I_b$, $I_c$.

Fig. 18 Steady-state experimental waveforms (120Vrms, 2kW) with PI compensation (with VFF and DFF, without ZSS injection): (a) phase-voltage $V_{a0}$, (b) phase currents $I_a$, $I_b$, $I_c$.

Fig. 19 Steady-state experimental waveforms (120Vrms, 2kW) with PI compensation (with VFF, DFF and, ZSS injection): (a) phase-voltage $V_{a0}$, (b) phase currents $I_a$, $I_b$, $I_c$.

Fig. 20 Steady-state experimental waveforms (120Vrms, 2kW) with PI compensation (with VFF, DFF and, ZSS injection): (a) phase-voltage $V_{a0}$, (b) phase currents $I_a$, $I_b$, $I_c$. 

\[ THD_a = 2.78\% \quad PF_a = 0.9988 \]
\[ THD_b = 3.11\% \quad PF_b = 0.9983 \]
\[ THD_c = 2.82\% \quad PF_c = 0.9976 \]

\[ THD_a = 2.82\% \quad PF_a = 0.9982 \]
\[ THD_b = 3.08\% \quad PF_b = 0.9987 \]
\[ THD_c = 2.75\% \quad PF_c = 0.9982 \]

\[ THD_a = 5.48\% \quad PF_a = 0.9951 \]
\[ THD_b = 4.83\% \quad PF_b = 0.9564 \]
\[ THD_c = 4.86\% \quad PF_c = 0.9976 \]

\[ THD_a = 5.70\% \quad PF_a = 0.9982 \]
\[ THD_b = 6.49\% \quad PF_b = 0.9983 \]
\[ THD_c = 4.73\% \quad PF_c = 0.9983 \]
available for compensation of various parameter mismatches and offset errors.

It is also shown that the DFF, in addition to reducing the phase shift between the respective input voltages and currents in the implementation with PI compensation, significantly improves the effectiveness of VVF in improving the output-voltage transient response with respect to input-voltage changes in the P-compensation implementation. This behavior of the current controller with P compensation is the result of the variation of the voltage-controller output \( v_{E_A}^* \) with the changes of the input-voltage amplitude. Without DFF, \( v_{E_A}^* \) varies with the square of the input-voltage amplitude, whereas, with DFF, \( v_{E_A}^* \) is independent of the input-voltage amplitude.

Finally, it is shown that ZSS injection improves the THD of input-currents in current controllers with both PI and P compensation. This is the result of the reduced peak-to-peak ripple in the inductor currents around the peak values of the phase voltages. In addition, ZSS injection increases the margin in the linear operation range for compensation of various parameter mismatches and offset errors.

APPENDICES

APPENDIX A - CONTROLLER DESIGN

In the design of the voltage and current controllers, the digital redesign approach is used, i.e., the controllers are designed in continuous-time domain (s-domain) and then translated to discrete-time domain (z-domain) which can be handled by the DSP. Since to achieve low distortions of the input currents, the voltage-loop (outer-loop) bandwidth must be well below the line frequency, whereas the current-loop (inner-loop) bandwidth should be in the kHz range, the control loops are well separated so that they can be independently designed. The faster current loop is designed first assuming that the voltage loop is open and then the slow voltage loop is designed by considering the boost power stage with the current loop closed to be a new plant.

A. Current-Controller Design

For the three-phase-rectifier-control implementation with three independent current controllers, the design of the phase-current controllers reduces to the single-phase design. The equivalent continuous-time small-signal block diagram of the phase-current loop is shown in Fig. A1, which is obtained directly from the block diagram in Fig. 1 assuming that the voltage loop is open, i.e., \( v_{E_A}^* = 0 \), and that for several switching cycles the input phase voltage can be considered constant, i.e., \( v_{x_i}^* = 0 \), where \( x \in \{a,b,c\} \). In Fig. A1, \( G_i(s) \) is the duty-cycle-to-inductor-current transfer function, \( G_{LPP}(s) \) is the current-sensing low-pass filter transfer function, \( G_{CC}(s) \) is the phase-current controller transfer function, \( 1/C_{pk} \) is the gain of the digital PWM, and \( 1/FSR \) is the gain of the ADC converter. The current loop in Fig. A1 also includes delay time \( T_{DLY} \), which consists of the transport delay (delay from the instant the inductor currents are sampled at the peak of the triangular carrier to the instant the duty cycle is updated at the beginning of the next switching cycle) \( T_{DLY,\text{Transport}} = T_{sw}/2 \), where \( T_{sw} \) is the switching period, and the PWM delay of the triangular carrier \( T_{DLY,\text{PWM}} = T_{sw}/2 \). [26] Therefore, the total delay in the current loop is \( T_{DLY} = T_{sw} \).

Since the crossover frequency of the current loop is relatively high (typically greater than 1-2 kHz), transfer function \( G_i(s) \) at frequencies around the crossover frequency of the current loop can be approximated as

\[
G_i(s) \approx \frac{V_o}{sL} = \frac{\omega_{id}}{s}, \quad (A1)
\]

where \( \omega_{id} = V_o/L \). Then, the plant transfer function is obtained as

\[
G_{PL,i}(s) = \frac{1}{C_{pk}} G_i(s) \cdot K_{cs} \cdot G_{LPP}(s) \cdot \frac{1}{FSR} e^{-sT_{DLY}} = \frac{K_{ci}}{FSR C_{pk} s} \frac{1}{1 + \frac{s}{\omega_{id}}} e^{-sT_{DLY}}, \quad (A2)
\]

where, \( \omega_{id} = 2\pi f_{PP} \) is the corner frequency of the low-pass filter.

To facilitate the explanation of the current controller design, Bode plots of transfer functions \( G_i(s) \), \( G_{PL,i}(s) \), and \( G_{CI}(s) \), as well as loop-gain transfer function \( T(s) \) are shown in Figs. A2(a) and A2(b) for P and PI compensation, respectively. To achieve a 45° phase margin, the current-loop bandwidth \( f_{CI} \) with P and PI compensation is selected as 2.5 kHz and 2 kHz, respectively.

For the P compensation, gain of the current-controller \( K_{pl,P} \) is

\[
K_{pl,P} = \left| G_{CC,P}(f_{CI,P}) \right| = \frac{1}{\left| G_{PL,P}(f_{CI,P}) \right|} = 3337, \quad (A3)
\]

whereas, for the PI compensation, proportional gain \( K_{pl,PI} \) is

\[
K_{pl,PI} = \left| \frac{G_{CC,P}(f_{CI,P})}{G_{PL,P}(f_{CI,P})} \right| = \frac{1}{\left| G_{PL,P}(f_{CI,P}) \right|} \left| 1 + \left( \frac{f_{ZCC}}{f_{CI,P}} \right)^2 \right| = 2640, \quad (A4)
\]

and integral gain \( K_{II,PI} \) is

\[
K_{II,PI} = 2\pi f_{ZCC} K_{pl,PI} = 4976282, \quad (A5)
\]

where the zero of PI compensation is selected \( f_{ZCC} = 300 \text{ Hz} \) < \( f_{CI,PI} \) to achieve 45° phase margin.
Translation from s-domain to z-domain is performed by bilinear (Tustin’s) approximation

\[ s = \frac{2}{T_s} \frac{z - 1}{z + 1}, \]

where, \( T_s = 1/f_i \) is the sampling period. Finally, the current controller parameters in z-domain are obtained as

\[ K_{plz,p} = K_{pl,p} = 3337 \] (A7)

for P compensation, and

\[ K_{plz,pl} = K_{pl,pl} = 2640 \] (A8)

and

\[ K_{ilz,pl} = K_{il,pl} = \frac{T_s}{2} = 124 \] (A9)

for PI compensation.

B. Voltage-Controller Design

The equivalent continuous-time small-signal block diagram of the voltage loop is shown in Fig. A3. Because the bandwidth of the voltage loop is very low, i.e., it is below the line frequency, the effect of time delays in the voltage loop is negligible. The low-frequency small-signal control-to-output-voltage transfer function \( G_{vc}(s) \) in Fig. A3 is derived in [28]. With resistive load \( R_{load} \), which was used in the presented experimental performance evaluation, \( G_{vc}(s) \) is given by [28]

\[ G_{vc}(s) = \frac{v_o}{V_{EA}} = g_C R_{load} \frac{1}{2 + \frac{1}{\omega_p V_{CV}}} \] (A10)

where,

\[ \omega_p V_{CV} = \frac{2}{C_o R_{load}} = \frac{2}{R_{load} \left( \frac{1}{C_p} + \frac{1}{C_n} \right)} \] (A11)

and \( g_C \) is the transconductance, defined in steady state as,

\[ g_C = \frac{I_{omax}}{V_{EAmax}} = 9.375 \text{ A/V}. \] (A12)

To provide an adequate margin for output-voltage low-frequency ripple and transients, the scaled value of \( V_{EA} \) is selected as \( V_{EAmax} = 0.8 \text{ V} \) at \( I_{omax} = P_{omax} / V_{nom} = 3000/400 = 7.5 \text{ A} \). Therefore, transconductance \( g_C \) is obtained as

\[ g_C = \frac{I_{omax}}{V_{EAmax}} = 9.375 \text{ A/V}. \] (A13)

The plant transfer function for the voltage loop is given as

\[ G_{PL,V}(s) = \frac{g_C K_d R_{load}}{2 \text{FSR}} \frac{1}{1 + \frac{s}{\omega_{AAF}}} \frac{1}{1 + \frac{s}{\omega_{pCV}}} \] (A14)

where, \( \omega_{AAF} = 2\pi f_{AAF} \) is the corner frequency of the anti-aliasing filter.

The design of the voltage controller with PI compensation is illustrated with Bode plots in Fig. A4. For low distortions of the input currents, the voltage-loop bandwidth \( f_{CV} \) is selected as 10 Hz.
The voltage-controller parameters are obtained as

$$K_{pV} = \frac{G_{CV}(f_{CV})}{1 + \left(f_{ZCV}/f_{CV}\right)^2} = 3.5$$  \hspace{1cm} (A15)

and

$$K_{iV} = 2\pi f_{ZCV}K_{pV} = 132 ,$$  \hspace{1cm} (A16)

where the zero is selected as \( f_{ZCV} = 6 \text{ Hz} < f_{CV} \), which results in a phase margin of 77\(^\circ\) >> 45\(^\circ\).

Finally, the voltage controller parameters in z-domain using the bilinear (Tustin’s) approximation are obtained as

$$K_{pVz} = K_{pV} = 3.5$$  \hspace{1cm} (A17)

and

$$K_{iVz} = K_{iV}\frac{T_z}{2} = 3.3\cdot10^{-3} .$$  \hspace{1cm} (A18)

APPENDIX B – INDUCTOR-CURRENT RIPPLE

Simulated waveforms of inductor current \( i_a \) around the positive peak of input phase voltage \( v_a \) in steady-state operation at nominal phase voltage of 120 Vrms and 2-kW load with P compensation (with VFF and DFF), for matched sensing gains and no offset errors in sensing, without and with ZSS injection are shown in Figs. B1 and B2, respectively. To better understand the ripple waveform of inductor current \( i_a \), the gate pulses of the bottom switches are also included in Figs. B1 and B2, whereas, the slope of inductor current \( i_a \) in different switching states is summarized in Table B1. The equivalent circuit for calculation of the slope of inductor currents is given in Fig. B3.

As shown in Figs. B1 and B2, for both cases (without and with ZSS injection), the peak-to-peak ripple of inductor current \( i_a \) is obtained during switching state ppp, where inductor current increases with slope \((v_a + v_{ZSS})/L\) (see Table B1).

Without ZSS injection, the duration of switching state ppp, \( T_{ppp1} \), is determined as

$$T_{ppp1} = T_{sw}\left(\frac{1}{2} - \frac{1}{2} \frac{V_m}{V_o}\right) .$$  \hspace{1cm} (B1)

Multiplying \( T_{ppp1} \) with the current slope

$$\left(\frac{di_a}{dt}\right)_o = \frac{V_o}{L} = \frac{V_m}{L}$$  \hspace{1cm} (B2)

at the positive peak of the phase voltage, the peak-to-peak ripple of inductor current without ZSS injection is obtained as

$$\Delta_{app} = \frac{T_{ppp1}}{2L f_{sw}}\left(1 - \frac{V_m}{V_o}\right) \hspace{1cm} (B3)$$

where, \( 1/f_{sw} = T_{sw} \).

With symmetrical ZSS injection [11], used in this paper, the duration of switching state ppp, \( T_{ppp2} \), is determined as

$$T_{ppp2} = T_{sw}\left(\frac{1}{2} - \frac{3}{4} \frac{V_m}{V_o}\right) .$$  \hspace{1cm} (B4)

TABLE B1 – SLOPE OF INDUCTOR CURRENTS

<p>| ( x=0 ) | ( x=V_a ) | ( x=V_b ) | ( x=V_c ) |</p>
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<th>( V_c )</th>
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<th>( V_{b0} )</th>
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<td>p</td>
<td>( V_a )</td>
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</tr>
</tbody>
</table>

*With ZSS injection, \( V_{a0} \) is replaced with \( V_{a0} + v_{ZSS} \)
Multiplying $T_{ppp}$ with the current slope

$$\left(\frac{di_n}{dt}\right)_n = \frac{v_{n0} + v_{ZSS}}{L} = \frac{3}{4} \frac{V_m}{L}$$  \hspace{1cm} (B5)

at the positive peak of the phase voltage, the peak-to-peak ripple of inductor current with ZSS injection is obtained as

$$\Delta I_{ppp} = \frac{3V_m}{8Lf_{sw}} \left(1 - 3 \frac{V_m}{2V_o}\right).$$  \hspace{1cm} (B6)

From Eqs. (B1)-(B6), it can be seen that with ZSS injection both the slope of inductor current $i_n$ and the duration of switching state $ppp$ are decreased compared to those without ZSS injection, which results in a decreased peak-to-peak ripple of the inductor current with ZSS injection compared to that without ZSS injection. Specifically, in this example, the slope of the inductor current is decreased 1.33 times and the duration of switching state $ppp$ is decreased 1.59 times, resulting in a total reduction of the peak-to-peak ripple of the inductor current approximately two times, which can also be seen in Figs. B1 and B2.

REFERENCES


