On-the-Fly Topology-Morphing Control — Efficiency Optimization Method for LLC Resonant Converters Operating in Wide Input- and/or Output-Voltage Range

Milan M. Jovanović, Fellow, IEEE, and Brian T. Irving

Abstract—This paper presents a control method for efficiency improvement of the LLC resonant converter operating with a wide input-voltage and/or output-voltage range by means of topology morphing, i.e., changing of power converter’s topology to that which is the most optimal for given input-voltage and/or output-voltage conditions. The proposed on-the-fly topology-morphing control maintains a tight regulation of the output voltage when topology transitions so that topology transitions are made without noticeable output-voltage transients. The performance of the proposed topology morphing method is verified experimentally on an 800-W LLC dc/dc converter prototype designed for a 100-V to 400-V input-voltage range.

Index Terms—De/Dc converters, LLC series resonant converter, wide range, efficiency optimization, topology morphing

I. INTRODUCTION

In many applications, power conversion circuits are required to operate with a wide input-voltage and/or output-voltage range. For example, a majority of single-phase ac/dc power supplies used in today’s computer and telecom power systems must operate in the universal ac-line range from 90 to 264 Vrms and provide constant- or variable-voltage regulated output(s). Typically, telecom ac/dc power supplies provide a regulated output between 42 V to 58 V, whereas power supplies for desktop, networking, and server applications deliver a constant-voltage with single or multiple output(s). However, to further improve the energy efficiency, single-output server power supplies with two-level selectable output voltage have been recently introduced. Specifically, these power supplies with dynamically adjustable output voltage deliver a 12-V output at full and mid-range loads, whereas at light loads their output voltage is reduced to 6 V to improve the light-load efficiency.

Ac/dc battery chargers are another major class of power converters that operate with a wide input- and output-voltage range. For example, the typical output-voltage range of today’s plug-in and battery electric vehicle (EV) on-board chargers is 200-450 V. At the same time, this is also the input-voltage range of on-board dc/dc converters that condition power between the high- and low-voltage batteries.

It is well understood that there is a strong trade-off between the input-voltage and/or output-voltage range and the conversion efficiency [1]-[8]. Power converters operating in a wide input-voltage and/or output-voltage range exhibit a larger efficiency fall-off than their narrow-range counterparts.

Generally, the detrimental effect of wide input and/or output voltage range on the conversion efficiency is more severe in resonant converters than in pulse-width-modulated (PWM) converters. Namely, the resonant converters most commonly regulate the output voltage by changing the switching frequency, i.e., by moving the operating point away from the resonant frequency as the input voltage increases and/or output voltage decreases. As a result, they suffer from progressively increased losses as the input- and/or output-voltage range is widened. This is the major reason that resonant dc/dc converters, including the most efficient series-resonant LLC converter topology, are not able to maintain high efficiency across the entire range when input-voltage or output-voltage range is wide.

The overall efficiency of converters operating in wide input-voltage and/or output-voltage range, can be improved by multi-stage conversion [9]-[12]. Typically, in this approach, the regulation task and isolation task are performed in two separate stages, i.e., the first stage is used for regulation, whereas the second stage for isolation. Because the isolation stage is unregulated [9], [11], [12], or semi-regulated [10], i.e., regulated in a very narrow range, its efficiency can be maximized. While this approach has been demonstrated to improve efficiency compared to a single-stage converter, its major drawback is increased number of components which increases the circuit’s complexity and cost.

Another approach to deal with very wide input-voltage and/or output-voltage range is to employ topology morphing, i.e., a topology change. By changing the topology, the gain of the converter is changed which narrows the effective range that the converter needs to be optimized for, thus, improving efficiency. Several topology-morphing techniques are reported in [13]-[17]. Specifically, in [13], a 3-level half-bridge (HB) LLC converter is modulated as a 2-level converter when the input voltage is in the upper range, whereas for lower-range input voltages it is modulated as a 3-level converter. In [14], the conventional 2-level full-bridge (FB) LLC topology is used in the low-input range and it is changed to the half-bridge...
(HB) topology when operating in the upper-voltage range. The idea in [14] is further expanded in [15]-[17] by employing two transformers. The major deficiency of the on-the-fly topology-morphing approaches described in [13] and [14] is that the topology transitions are made abruptly so that the output exhibits severe overshoots and undershoots during the transitions. In the approaches in [15]-[17], topology transitions are made by briefly stopping and then soft-restarting the circuit, i.e., by interrupting the power flow, which also results in large output-voltage transients that may be reduced by significantly increasing the output filter capacitance. Both of these transition methods are not desirable in applications that require tight regulation of the output voltage at all times.

In this paper, a method of on-the-fly topology morphing of the LLC resonant converter operating with a wide input-voltage and/or output-voltage range that does not exhibit significant voltage transients and does not require increased energy storage components is described. In this approach, the LLC topology is gradually changed between the full bridge (FB) and half bridge (HB) so that a tight output control and uninterrupted power flow are maintained during the transitions. The performance of the proposed topology morphing method is verified on a 48-V, 800-W LLC dc/dc converter designed for a 100-V to 400-V input-voltage range.

II. DESIGN TRADE-OFFS OF LLC CONVERTER

To facilitate the explanation of LLC converter’s design trade-offs in applications with wide-input and/or output-voltage range, Figs. 1(a), (b), and (c) show the full-bridge (FB) LLC converter, its fundamental-frequency equivalent circuit, and the dc voltage-conversion ratio, respectively [18], [19]. The FB LLC converter in Fig. 1(a) utilizes magnetizing inductance \( L_M \) as a part of the resonant-tank circuit that also includes \( L_R - C_R \) series-resonant branch.

Generally, the LLC converters employ variable switching-frequency control to regulate the output against input-voltage and load-current changes. This frequency control is implemented by operating the switches with approximately 50% duty cycle and providing a small dead time between the commutations of the complementary same-leg switches to achieve zero voltage switching (ZVS). A wider input-voltage and/or load-current range requires a wider switching-frequency range. Generally, a wide switching-frequency range is not desirable because it has a detrimental effect on the performance of the converter. For a given input-voltage and load-current range, the frequency range is dependent on the value of transformer’s magnetizing inductance \( L_M \). In series-resonant LLC converters, magnetizing inductance \( L_M \) is essential in enabling the converter operation at very light and no load by providing a resonant-current path when the load is small or zero. By decreasing magnetizing inductance \( L_M \), i.e., by increasing the magnetizing current relative to the primary-referred load current flowing through resistor \( n^2R_{ac} \) shown in Fig. 1(b), the frequency range is reduced since with a reduced magnetizing inductance the converter starts becoming more as a parallel resonant converter. However, since the magnetizing current does not flow through the load, as illustrated in Fig. 1(b), it represents a circulating current which unnecessarily generates conduction loss in the primary switches and the transformer. Therefore, because of a strong tradeoff between the frequency range and primary-side circulating current loss, a proper selection of the magnetizing inductance value is of the utmost importance for optimizing the efficiency of the LLC converter. Typically, for given values of series resonant circuit components \( L_R \) and \( C_R \) that determine the series resonant frequency \( f_0 = 1/\sqrt{L_R C_R} \) in Fig. 1(c), the optimal performance is obtained by selecting the magnetizing inductance so that the ratio \( L_M/L_R \) is maximized.

As illustrated in the dc-conversion characteristics in Fig. 1(c), the circulating current increases as the frequency decreases and Q-factor decreases, whereas the switching losses increase with the increasing frequency. The optimal balance between the circulating-current and switching loss occurs around the series resonant frequency \( f_0 \) where LLC converters exhibit the maximum efficiency. In fact, the LLC converter exhibits an unmatched efficiency when implemented
as a dc/dc transformer, i.e., when it operates without a regulation loop at a constant frequency close to the series-resonant frequency of the resonant tank [12].

To further explain tradeoffs in designing the LLC converter for a wide input- and/or output-voltage range, Figs. 2(a) and (b) show the dc-voltage conversion of the LLC converter along with minimum and maximum gain lines that correspond to a 1.5:1 and 3:1 gain (i.e., input and/or output voltage) range, respectively. As it can be seen from Figs. 2(a) and (b), since the choice of minimum gain $M_{\text{MIN}}$ is limited to values around unity to provide light/no-load output-voltage regulation, the design for the wide range converter in Fig. 2(b) has a lower minimum frequency and a significantly lower minimum Q-factor when operating at the maximum output and minimum input voltage i.e., at $M_{\text{MAX}}$. As a result, the wide-range (3:1) converter exhibits significantly lower efficiency compared to that of its narrow-range (1.5:1) counterpart due to increased circulating-current conduction losses.

The efficiency of the LLC converter operating in a very wide input-voltage and/or output-voltage range can be improved by recognizing that for the same values of the turn-ratio of the transformer $n = N_P/N_S$ and resonant-tank components $L_0$, $C_0$, and $L_R$, the dc voltage gain of the FB LLC topology is twice as large as that of the half-bridge (HB) LLC topology, as illustrated in Fig. 3. As a result, the FB LLC topology is the optimal choice for a range of operating conditions where the dc voltage gain is high, i.e., where the input voltage is in the low range and/or output voltage is in the high range, whereas the HB LLC topology is more suitable for a range of the input and/or output voltage exhibiting a low dc voltage gain.

Specifically, for the 3:1-range example, the efficiency of the LLC converter can be improved by operating the converter as the FB LLC in the high-gain range, i.e., for gain $M$ between 1.5 and 1, and operating it as the HB LLC in the low-gain range, i.e., for $M$ between 1 and 0.5. Because of the power-stage gain change due to the topology change at $M = 1$, the converter can be designed for a gain range that is only one half of the specified range. As a result of a very much reduced operation range, the efficiency fall-off of the LLC converter with topology changing (morphing) is much less than that of its fixed-topology counterpart. It should be noted that the topology transition does not need to occur exactly at $M = 1$. Depending on a specific design, it may be optimal to make a transition slightly above or below the unity gain. In fact, the best approach to determine the optimal topology transition gain is to measure the efficiency of the converter in both the FB and HB mode and take the gain where the efficiencies of the FB and HB circuit are equal as the transition gain.

III. PROPOSED ON-THE-FLY MORPHING CONTROL

Since the HB LLC topology can be obtained from the FB LLC topology by not switching one leg of the HB LLC converter, i.e., by permanently keeping one switch in the non-switching leg on and the other switch off, the performance optimization of the LLC converter operating in a very wide input-voltage and/or output-voltage range can be obtained with a proper control.

In its simplest form, the on-the-fly controller which provides transitions between the FB and HB LLC topology and vice versa can be implemented so that the modulation of one leg of the bridge is abruptly stopped and restarted [14]. Generally, this approach is not acceptable in applications that require a tight regulation of the output at all times. Namely, because in the FB LLC the steady-state average (dc) voltage of resonant capacitor $V_{C_{av}}^{FB} = 0$, whereas in the HB LLC circuit $V_{C_{av}}^{HB} = V_{IN}/2$, an abrupt topology change causes a large initial imbalance of the transformer and resonant inductor volt-seconds, which besides the potential to saturate these components, creates a significant imbalance between the input power and output power. Since the control loop speed (bandwidth) is not fast enough to correct for this abrupt transient power imbalance, the output voltage exhibits unacceptably large transients (under and overshoots). Generally, these transients can be reduced by increasing the energy storage in the output filter, i.e., by significantly increasing the output capacitance of the LLC converter. However, this approach is not only undesirable because of increased cost, but in high-power density applications it is not practical because it requires increased volume.

To minimize and even eliminate output-voltage transients, as well as possible magnetic component saturation, it is necessary to implement a gradual topology transition.
Generally, the topology transition time must be long enough to allow the control loop to maintain a tight regulation of the output during the transition.

The on-the-fly transition control from the FB topology to the HB topology proposed in this paper is illustrated in Fig. 4. During the FB operation, all switches are operated with variable switching frequency and 50% duty ratio. During the transition, switches S1 and S2 continue to operate with variable switching frequency and 50% duty ratio to maintain the output at the desired level, whereas switches S3 and S4 are PWM modulated and frequency modulated so that the duty ratio of S3 is monotonically increased from 50% to 100% and the duty ratio of S4 is reduced from 50% to 0% in a complementary fashion. Since at the end of the transition period switch S3 is permanently on and switch S4 permanently off, the converter continues to operate as the HB converter with variable-frequency control of switches S1 and S2. During the transition from the HB to the FB topology, switches S1 and S2 are modulated in the opposite direction, i.e., the duty ratio of switch S1 is decreased from 100% (continuously on) to 50%, whereas at the same time the duty ratio of S2 is increased from 0% (continuously off) in a complementary fashion. With this topology-transition control, tight output regulation is maintained at all times by frequency regulation of switches S1 and S2.

In the morphing control in Fig. 4, the turn-on instants of switches S1 and S3 are synchronized during the topology transition periods. However, it should be noted that other synchronization methods are possible such as, for example, the turn-on-instant synchronization of switches S2 and S4.

Implementation of the proposed topology morphing control can be either analog or digital. However, a digital implementation is preferred since today’s DSPs offer adequate performance and flexibility to implement a reliable topology morphing control that requires simultaneous frequency and duty-cycle modulation. Figure 5(a) shows the block diagram of digital implementation of the controller that is used in the experimental prototype circuit reported in Sec. VI, whereas Fig. 5(b) illustrates its key waveforms during the FB-to-HB transition.

In the implementation in Fig. 5(a), the duty cycles of switches S1-S4 are obtained by digital pulse-width modulator (PWM), i.e., by using a digital carrier ramp that is generated by counting DSP clock periods $T_{CLK}$. Since the carrier ramp period $T_s=N_{CAR}T_{CLK}$, where $N_{CAR}$ is the number of clock periods, carrier frequency $f_s$ is proportional to $1/N_{CAR}$. As illustrated in Fig. 5(a), the ramp frequency is set by the voltage-controlled oscillator (VCO) based on output of the voltage controller $V_{EA}$ which processes the error between measured output voltage $V_{O(REF)}$ and its reference $V_{O(SEN)}$. The VCO transfer function is set by the selection of its maximum frequency, i.e., minimum count number $N_{MIN}^{CAR}$ and gain $K_{VCO}$. As shown in Fig. 5(a), $N_{CAR}$ is obtained by calculating the reciprocal value of the VCO output, $1/N_{CAR}$.

The control signals for complementary switches S1 and S2 that always operate with the 50% duty cycle are obtained by comparing the ramp with one-half of its count value $N_{CAR}$, i.e., with $0.5N_{CAR}$, as shown in Fig. 5(a) and illustrated in Fig. 5(b). The duty cycles of the complementary morphing switches S1 and S4 are obtained by comparing the carrier ramp with $0.5N_{CAR}+N_{TRANS}$, where $N_{TRANS}$ is the output of the transition-time-control counter. The range of this up-and-down counter is limited between zero and $MAX=0.5N_{CAR}$. The topology transition time is adjusted by counter update period $T_{COUNTER}$, which is selected to be a multiple of sampling period $T_{SAMPL}$, i.e., $T_{COUNTER}=kT_{SAMPL}$. Since transition time $T_{TRANS}$ is
equal to the time required to count \(0.5N_{\text{CAR}}\) counter periods \(T_{\text{COUNT}}\), i.e., since \(T_{\text{TRAN}}=0.5N_{\text{CAR}}T_{\text{SAMPLE}}\), \(k\) can be determined as \(k = 2T_{\text{TRAN}}/(N_{\text{CAR}}T_{\text{SAMPLE}})\). In Fig. 5(a), the counter update period is modeled by delay block \(z^{-k}\). The value of \(N_{\text{TRAN}}\) and counting direction is controlled by output of the transition trigger circuit \(V_{\text{TRIG}}\) that compares sensed input voltage \(V_{\text{INSENS}}\) with desirable topology-transition voltage \(V_{\text{INTRAN}}\). When \(V_{\text{INSENS}}>V_{\text{INTRAN}}\), i.e., when the converter is supposed to work in the FB mode, \(V_{\text{TRIG}}\) is high and counter is set up to count down. As a result, in steady-state, counter value \(N_{\text{TRAN}}\) is equal to zero, i.e., \(N_{\text{TRAN}}=0\), so that switches \(S_3\) and \(S_4\) also operate with 50% duty cycle, as illustrated in Fig. 5(b). When \(V_{\text{INSENS}}<V_{\text{INTRAN}}\), \(V_{\text{TRIG}}\) is low and counter is set up to count up. In steady-state, the counter value reaches its maximum limit \(N_{\text{TRAN}}=\text{MAX}=0.5N_{\text{CAR}}\), so that the output of comparator COMP3 stays permanently high since the positive input of the comparator is equal to the ramp count, i.e., \(0.5N_{\text{CAR}}+N_{\text{TRAN}}=N_{\text{CAR}}\). As a result, switch \(S_3\) is permanently on and switch \(S_4\) is permanently off and the converter operates in the HB mode, as illustrated in Fig. 5(b).

The topology morphing transitions are initiated every time signal \(V_{\text{TRIG}}\) changes state. As shown in Fig. 5(b), the FB-to-HB transition starts after \(V_{\text{TRIG}}\) changes from high-to-low. This \(V_{\text{TRIG}}\) change triggers the transition-time-control counter to start counting up from zero to \(\text{MAX}=0.5N_{\text{CAR}}\) which increases the duty cycle of switch \(S_1\) from 50% toward 100% and at the same time reduces the duty cycle of complementary switch \(S_2\) from 50% towards zero. Similarly, the HB-to-FB transition, not shown in Fig. 5(b), is initiated every time signal \(V_{\text{TRIG}}\) changes from low to high. Finally, it should be noted that in Fig. 5(b) the transition-time-control counter is updated every switching cycle, i.e., \(T_{\text{COUNT}}=T_{\text{SAMPLE}}=T_s\), for the sake of simplifying the drawing.

As it can be seen from Fig. 5(b), the topology-morphing control is completely decoupled from the output-voltage feedback control loop, i.e., the output-voltage feedback control loop that is established through error amplifier EA and VCO regulates the output at all times by frequency control of switches \(S_3\) and \(S_4\), irrespective of the state of morphing-leg switches \(S_1\) and \(S_2\). As a result, the proposed topology morphing control makes it possible to transition between the two topologies without significant output transients.

### IV. Analysis of Operation During Topology Transition

Because during the topology transition periods the converter in Fig. 1(a) operates with asymmetrical duty cycles of switches \(S_3\) and \(S_4\), its operation is different than that with

![Digital implementation of proposed topology morphing control](image-url)
symmetrical duty cycles. In fact, for small duty-cycle asymmetries, i.e., for switch S1 duty cycle $D_{S1}$ approximately $D_{S2} < 0.6$, the operation of the circuit is still the same as that of the conventional FB LLC converter with symmetrical duty cycles, i.e., with $D_{S2} = 0.5$. As a result, the properties of the FB LLC converter operating with $D_{S2} < 0.6$ are the same as that of its counterpart controlled by symmetrical duty cycles of the switches, i.e., all primary switches are turned-on with ZVS. However, for duty cycles $D_{S2} > 0.6$, the ZVS property of morphing-leg switches $S_1$ and $S_4$ is lost during the topology-transition period.

To facilitate the explanation of the converter during topology-transition periods, Fig. 6 shows a simplified circuit diagram of the FB LLC converter with the secondary-side full-bridge diode rectifier along with reference directions for its key voltages and currents. The analysis is carried out for the full-bridge diode-rectifier secondary to enable direct waveform comparisons with that of the experimental circuit that is presented in Sec. VI. It should be noted that the same analysis and conclusions are also applicable to the full-bridge secondary-side rectifier implementation with synchronous rectifiers, as well as to the secondary-side implemented with center-tap transformer either with diode or synchronous rectifiers.

In Fig. 6, the output voltage ripple is neglected by modeling the output filter capacitor with constant voltage source $V_O$, whereas the steady-state dc-voltage of the resonant capacitor is modeled by voltage source $V_{C_{(av)}}$. Voltage $V_{C_{(av)}}$ depends on duty cycle $D_{S2}$ and can be calculated as

$$V_{C_{(av)}} = (D_{S2} - 0.5)V_{IN} \quad (1)$$

by recognizing that in steady-state the average voltage across the resonant inductor and transformer windings must be zero. As expected, the average-voltage of the resonant capacitor during the transition period varies between zero when the converter operates as the FB LLC, i.e., for $D_{S2} = 0.5$, and $V_{IN}/2$ when the converter operates as the HB LLC, i.e., for $D_{S2} = 1$.

Figures 7 and 8 respectively show the key waveforms and topological stages for operation with asymmetrical duty cycle $D_{S2} = 0.75$. As can be seen from Figs. 7 and 8(a), before primary switches are commutated at $t = T_0$, the negative resonant current $i_L$ and magnetizing current $i_M$ are carried by the conducting diagonal pair of switches $S_2$ & $S_3$, whereas secondary current $i_S$ that is the same as output current $i_O$ and equal to $i_S = i_O = nI_P = n(i_L - i_M)$ is carried by rectifiers $D_{R1} & D_{R4}$. At $t = T_0$, after switches $S_2$ & $S_4$ are turned off and switches $S_1$ & $S_3$ turned on (with a small delay to achieve ZVS, not shown in Fig. 7), the resonant current that continues to flow in the same direction is commutated from switches $S_2$ & $S_4$ to switches $S_1$ & $S_3$, as shown in Fig. 8(b). This stage ends at $t = T_1$ when resonant current $i_L$ becomes equal to magnetizing current $i_M$ so that primary current $i_O$ and, consequently, secondary current $i_S$ becomes zero. Because at $t = T_1$ secondary current $i_S$ changes direction from negative to positive, it commutates from rectifiers $D_{R2} & D_{R4}$ to rectifiers $D_{R1} & D_{R3}$, as illustrated in Fig. 8(c). This stage ends at $t = T_2$ when resonant current $i_L$ becomes zero. From $t = T_2$, resonant current $i_S$ continues to flow through switches $S_1$ & $S_3$ in the positive direction, as shown in Fig. 8(d). During this stage, magnetizing current $i_M$ changes sign, i.e., it becomes positive after $t = T_{22}$, which is shown by the dashed magnetizing current arrow in Fig. 8(d). This stage ends at $t = T_3$ when switch $S_3$ is turned off and its complementary same-leg switch $S_2$ is turned on, as shown in Fig. 7. After switch $S_1$ is turned off, positive resonant currents $i_L$ continues to flow through switch $S_2$, as shown in Fig. 8(e). At $t = T_4$, decreasing resonant current $i_L$ becomes equal to magnetizing current $i_M$ making both the primary and secondary current zero. If for the given design the absolute value of the voltage across the transformer secondary $|V_S| = [-L_MV_{C_{(av)}}/(n(L_M + L_R))]$ is greater than output voltage $V_O$, i.e., if $|V_S| > V_O$, the primary and secondary current will change sign and the negative secondary current will flow through rectifiers $D_{R2} & D_{R4}$, as

![Fig. 6. Simplified circuit diagram of FB LLC converter with full-bridge secondary-side diode rectifier showing reference directions of key voltages and currents.](image)

![Fig. 7. Key waveforms of FB LLC converter in Fig. 6 for $D_{S2}=0.75$.](image)
shown in Fig. 8(f). When at $t = T_3$, resonant current $i_R$ reaches zero, it continues to flow in the negative direction through switch $S_2$ and antiparallel diode of switch $S_1$, as shown in Fig. 8(g). During this stage, magnetizing current $i_M$ changes sign, i.e., it becomes negative after $t = T_{55}$, which is shown by the dashed magnetizing current arrow in Fig. 8(g). Since switch $S_3$ current reaches zero at $t = T_5$, i.e., before the switch is turned off at $t = T_6$, switch $S_3$ operates with zero-current switching (ZCS). As a result, when at $t = T_6$ switch $S_1$ is turned off and switch $S_3$ turned on, i.e., at the very beginning of the stage in Fig. 8(h), the antiparallel diode of switch $S_1$ exhibits reverse-recovery current $I_{RR}$, as shown in Fig. 8(h). This reverse-recovery current causes additional switching losses on switches $S_1$ & $S_4$, which are negligible because of a relatively short topology-transition time, but more importantly it may generate switching noise that may upset the control circuit. The stage in Fig. 8(h) ends at $t = T_7$ when a new switching cycle is initiated by turning off switches $S_2$ & $S_4$ and turning on switches $S_1$ & $S_3$.

It should be noted that because of asymmetrical duty cycles of the switches in the transition leg, secondary current is also asymmetrical which introduces a dc component of magnetizing current $i_{M_{(av)}}$, as shown in Fig. 7.

It also should be noted that if the absolute value of secondary voltage $V_S$ at $t = T_4$ when resonant current $i_L$ reaches zero is not greater than output voltage $V_O$, i.e., if $|V_S| < V_O$, the secondary current will stay at zero until switches $S_1$ & $S_4$ are commutated at $t = T_6$ since secondary-side rectifiers will be reversed biased. As a result, in this mode of operation, during the $[T_4 - T_5]$ interval rectifier voltage $V_{DRI1}$ is $0.5V_O$ instead of $V_O$ and inductor current $i_L$ is equal to magnetizing current $i_M$, as indicated by the red line segments in Fig. 7.

Finally, one more mode of operation may occur at large duty cycles, i.e., for $D_{C2} > 0.9$, when positive resonant current $i_L$ becomes equal to magnetizing current $i_M$, i.e., positive secondary current reaches zero, before switches $S_1$ & $S_2$ are commutated at $t = T_4$ and/or negative resonant current $i_L$ becomes equal to magnetizing current $i_M$, i.e., negative secondary current reaches zero, before switches $S_3$ & $S_4$ are commutated at $t = T_6$. In this mode, which is not shown in Fig. 7, the secondary side rectifiers are off during the periods the secondary current reaches zero and the subsequent commutation of the switches.

V. DESIGN CONSIDERATIONS

Generally, the performance optimization of the LLC converter with topology morphing follows a well-established
LLC-converter design procedure [2]-[7], [18]-[21]. Specifically, in the LLC converter with topology morphing, the values of series-resonant tank components $L_R$ and $C_R$, as well as the value of magnetizing inductance $L_M$ and turns ratio $n$ of the transformer are selected so that the performance of the circuit is optimized in the respective narrow gain (input/output voltage) range that it works either as the FB or HB converter.

The only major design difference between the conventional and topology-morphing implementation is that the latter one cannot be implemented with magnetically-coupled gate drive of the primary switches in the topology-transition leg $S_3-S_4$ because switch $S_1$ must permanently stay on while the converter operates as the HB LLC. As a result, the topology-transition leg must employ a high-side driver, as shown in the experimental circuit in Fig. 11. While the other primary leg does not require a high-side drive because it is continuously modulated, it is a good practice to also use a high-side drive in this leg to maintain primary-side symmetry.

To prevent any noise-related problems that may arise during topology-transition periods because of the reverse-recovery current of the body diode of switch $S_3$, it is advisable to employ magnetic beads in the drain and gate of switch $S_3$ to reduce the reverse-recovery current. Although not necessary, it is also a good practice to employ beads in all primary switches to maintain circuit symmetry or, at least in both transition-leg switches as illustrated in Fig. 11.

Since the operation with asymmetrical duty cycle introduces magnetizing-current dc-bias $i_{M(\text{av})}$ during transition periods, as shown in Fig. 7, it is necessary to examine the effect of this transient dc-bias on the operation of the transformer. Because an analytical expression for transient magnetizing current dc-bias is difficult to derive, simulations of the experimental circuit in Fig. 11 were used to quantify and evaluate the dc-bias effect. The first step in this simulation-based analysis was to establish a reference level for this evaluation by finding the maximum steady-state peak value of magnetizing current when the circuit operates either as the HB or FB converter. By using SIMPLIS simulation software, maximum steady-state peak value of magnetizing current $i_{M(\text{PEAK})}^{\text{MAX}}$ was determined by sweeping the respective input-voltage range, i.e., the 100-240-V range for the FB topology and the 240-400-V range for the HB topology. As expected, it was found that $i_{M(\text{PEAK})}^{\text{MAX}} = 8\, \text{A}$ occurs at minimum input voltage of 100 V, i.e., when the circuit operates as FB, because at this operating point the switching frequency is lowest, as can be seen from Fig. 12. Because of symmetrical operation in steady state, the minimum steady-state valley value of magnetizing current is $i_{M(\text{VALLEY})}^{\text{MIN}} = -i_{M(\text{PEAK})}^{\text{MAX}} = -8\, \text{A}$. Next, the average magnetizing current $i_{M(\text{AV})}^{\text{TRAN}}$, peak magnetizing current $i_{M(\text{PEAK})}^{\text{TRAN}}$, and valley magnetizing current $i_{M(\text{VALLEY})}^{\text{TRAN}}$ during topology-transition period are calculated as functions of duty cycle $D_{S3}$. Figure 9 shows the calculated $i_{M(\text{AV})}^{\text{TRAN}}$, $i_{M(\text{PEAK})}^{\text{TRAN}}$, and $i_{M(\text{VALLEY})}^{\text{TRAN}}$ for full-load transition at transition voltage $V_{\text{IN}}^{\text{TRAN}} = 240\, \text{V}$. Also superimposed on the plot in Fig. 9 are the lines for steady-state maximum peak magnetizing current $i_{M(\text{PEAK})}^{\text{MAX}} = 8\, \text{A}$ and minimum valley magnetizing current $i_{M(\text{VALLEY})}^{\text{MIN}} = -8\, \text{A}$. As can be seen from Fig. 9, transient magnetizing-current dc-bias $i_{M(\text{AV})}^{\text{TRAN}}$ changes from positive to negative as $D_{S3}$ increases and reaches a negative maximum of approximately $-4.5\, \text{A}$ when $D_{S3}$ is approximately 0.92. During the topology transition period, peak magnetizing current $i_{M(\text{PEAK})}^{\text{TRAN}}$ stays within the steady-state range. However, the value of valley magnetizing current $i_{M(\text{VALLEY})}^{\text{TRAN}}$ exceeds the maximum steady-state value of $-8\, \text{A}$ for duty cycles between 0.85 and 0.95. The magnetizing current reaches its absolute minimum value of around $-13.5\, \text{A}$ for duty cycle $D_{S3}$=0.92. This value is about 70% larger than that in the steady state so this transient increase of the transformer maximum current must be taken into account when designing the transformer.

Finally, the most important design step is to properly determine topology-transition time $T_{\text{TRAN}}$. To maintain acceptably small output-voltage transients (overshoots and undershoots), the rate of the duty-ratio change of switches $S_2$ and $S_3$ during the topology transition must be limited to that which allows the control loop to maintain full regulation. The optimal choice of transition time $T_{\text{TRAN}}$ and output-loop bandwidth $f_{\text{BW}}$ was found to be $T_{\text{TRAN}}/f_{\text{BW}} > 50 - 100$. For example, for the control-loop bandwidth of 1.2 kHz, the transition time can be as fast as 50-100 ms. It should be noted that during the topology-transition periods, small-signal control-to-output transfer function $G_{VC}$ changes with duty cycle $D_{S3}$, as illustrated in Fig. 10 which shows the full-load Bode plots of $G_{VC}$ of the experimental converter in Fig. 11 for different duty cycles $D_{S3}$ that are obtained by SIMPLIS simulations. As can be seen in Fig. 10, both the low-frequency ($<1\, \text{kHz}$) magnitude and transfer function order change during topology transitions. This behavior of $G_{VC}$ is in agreement with the results of small-signal analysis presented in [22]. Namely, since the dc-gain of $G_{VC}$ of the LLC converter is proportional to the slope of the dc-gain characteristic, the $G_{VC}$ dc-gain increases as the circuit makes a transition from the FB to the HB topology because, as illustrated in Fig. 3, at transition gain $M_{\text{TRAN}}$, the FB topology operates near the resonant frequency (operating point B) where the slope of the dc characteristic is small, whereas the HB topology operates at a frequency well below the resonant frequency (operating point C) where the slope of dc-
characteristic is steeper. In addition, as the switching frequency moves away from the resonant frequency during the topology transition from the FB to the HB topology, the $G_{VC}$ transfer function changes from the first order to the second order [22]. As a result, if a non-adaptive output-voltage control is employed, the transition time needs to be selected based on the worst-case, i.e., the minimum bandwidth. If necessary, an adaptive control that changes compensator parameters as a function of transition duty cycle to maintain optimum bandwidth during the topology transitions can be applied. This adaptive control can be easily and cost-effectively implemented with today’s microcontrollers and/or DSPs.

VI. EXPERIMENTAL PERFORMANCE EVALUATION

The performance of the proposed on-the-fly topology morphing control method is verified and evaluated on an 800-W LLC dc/dc converter designed for a 100-V to 400-V input-voltage range and an output voltage of 48 V. The circuit diagram of the power stage of the experimental prototype is shown in Fig. 11, whereas the specifications of key components are listed in Table I. For the selected components, the series-resonant frequency of the circuit is $f_0 = 98$ kHz. The control was implemented by TMS320F28027 fixed-point DSP with the control bandwidth at full load and low line set at 1 kHz by employing a three-pole, two zero compensator with gain $K = 12566$, poles $f_{p1} = 0$ Hz (integrator), $f_{p2} = 2$ kHz, and $f_{p3} = 8.2$ kHz and zeroes $f_{z1} = 500$ Hz and $f_{z2} = 700$ Hz. To implement the switching-frequency range from $f_S^{MIN} = 40$ kHz to $f_S^{MAX} = 300$ kHz with DSP’s clock frequency $f_{CLK} = 60$ MHz, the digital ramp limits were set to $N_{CAR}^{MIN} = f_{CLK}/f_S^{MIN} = 200$ and $N_{CAR}^{MAX} = f_{CLK}/f_S^{MAX} = 1500$. The gain of the VCO was set to -260 kHz/V.

![Fig. 10. Bode plots of small signal control-to-output transfer function $G_{VC}$ of experimental converter in Fig. 11 as a function of duty cycle $D_{S3}$ during topology transitions at $V_{IN} = 240$ V and full load $P_O = 800$ W.](image)

![Fig. 11. Experimental prototype.](image)

Table I: Components used in Experimental Circuit

<table>
<thead>
<tr>
<th>COMPONENT</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_R$</td>
<td>12 μH; ferrite core PQ26x25, 3C96; 8 turns of 0.1 mm x 40 Litz wire</td>
</tr>
<tr>
<td>$T_R$</td>
<td>Magnetizing inductance $L_{M1} = 71$ μH; Leakage inductance $L_{L1} = 0.57$ μH; Ferrite core PQ32x30, 3C96; $N_R/N_L = 3.75$; Primary: $N_R = 15$ using 0.1 mm x 180 Litz wire; Secondary: $N_L = 4$ using 5 mil Cu foil; Gap: 0.3 mm in outer legs</td>
</tr>
<tr>
<td>$C_R$</td>
<td>220 nF/ 1200 V, polypropylene</td>
</tr>
<tr>
<td>$C_{F1}$</td>
<td>13 x 2.2 nF/ 100 V, ceramic X7R</td>
</tr>
<tr>
<td>$C_{F2}$</td>
<td>1000 μF/ 63 V, electrolytic</td>
</tr>
<tr>
<td>$C_{F3}$</td>
<td>4 x 470 μF/ 63 V, electrolytic</td>
</tr>
<tr>
<td>$L_F$</td>
<td>0.68 μF; ferrite rod 19 mm x 8 mm, 6 turns of AWG10</td>
</tr>
<tr>
<td>$Q_L$</td>
<td>STW43N60FD 600 V/ 35 A</td>
</tr>
<tr>
<td>$D_{S3}$</td>
<td>30CPQ150 150 V/ 30 A</td>
</tr>
<tr>
<td>$D_{S1}$</td>
<td>M320F28027</td>
</tr>
<tr>
<td>$D_{S4}$</td>
<td>Si8233</td>
</tr>
<tr>
<td>$D_{S5}$</td>
<td>FairRite 266100</td>
</tr>
</tbody>
</table>

Figure 12 shows the measured full-load efficiencies of the experimental converter for both FB and HB topology. Due to the practical switching-frequency limitation of approximately 300 kHz, the FB converter could not regulate the output for input voltages higher than 270 V. It should be noted that the efficiency could have been maximized by employing synchronous rectifiers instead of the diode rectifiers.

It is interesting to note that the measured peak efficiency of the HB topology of approximately 94.3% is 0.5% higher than the measured peak efficiency of the FB topology of approximately 93.8% although both topologies operate with almost the same switching frequencies and resonant current magnitudes. This difference can be attributed to a lower loss of morphing-leg switches $S_3$ and $S_4$ when the circuit operates as the HB converter. Namely, in the HB topology switch $S_3$ is permanently off so it does not exhibit any losses, whereas switch $S_4$ is permanently on and exhibits only conduction loss due to the resonant current flow through the channel of the switch and, for high peak currents, simultaneous current flow through its body diode. Since in the FB topology switches $S_3$ and $S_4$ are continuously modulated, they exhibit both switching and conduction losses. In addition, since both switches prior to their respective turn-on instants carry the resonant current through the body diode to achieve ZVS, their conduction loss is further increased compared to the corresponding loss in the HB topology.

0885-8993 (c) 2015 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.
As can be seen in Fig. 12, to maximize the efficiency across the entire input-voltage range, the topology transition voltage is selected at the intersection of the FB and HB efficiency curves, i.e., at 240 V. With topology morphing, the worst-case (minimum) full-load efficiency in the entire 100-400-V range is determined by that at the minimum input voltage of 100 V, which is approximately 90.5%. If the FB were able to operate in the entire input-voltage range from 100-400 V, i.e., if the controller were able to provide required frequency range, the full-load efficiency at 400-V input would be very much below 90% as illustrated by the extrapolated efficiency line in Fig. 12. It should be noted that the efficiency dependence on the input voltage at partial load is similar to that at full load. As a result, at any load the optimum topology transition voltage can be determined and stored in a look-up table so that the topology morphing occurs at the most desirable input voltage at all loads.

To establish a reference for performance evaluation of the proposed topology morphing control, Fig. 13 shows the key waveforms during the full-load topology change at $V_{IN} = 200$ V with the topology morphing control disabled, i.e., for an abrupt topology change [14]. As it can be seen from Fig. 13, the output voltage at the topology-transition instants exhibits approximately 13-V, i.e., 27%, overshoot and undershoot, which for the majority of applications is far outside the specified limits.

Figure 14 shows the key waveforms during the full-load topology transition with the proposed topology morphing control enabled. As can be seen during the 80 ms transition periods, the output voltage transients are limited to below 0.43-V, i.e., 0.9%, which is more than 30 times lower compared to those without the topology morphing control. Specifically, the maximum positive deviation from the steady-state output voltage (overshoot) is 0.43-V, i.e., 0.9%, whereas maximum negative deviation (undershoot) is -0.34-V, i.e., -0.7%. During transitions, the peak of resonant current $i_L$ exceeds its steady-state value by approximately 50%, which is still well within the design margins of inductor $L_{GR}$. For a given control design, the overshoot and undershoot of the output voltage is smaller if the transition time is longer. As illustrated in Fig. 15, for the 500-ms transition time, the maximum transient deviation of the output voltage is only 0.14-V, i.e., 0.3%.

Fig. 12. Measured full-load efficiency of experimental converter for both full bridge and half bridge topology. Dashed-dot line shows extrapolated efficiency.

Fig. 13. Measured switch $S_3$ gate-to-source voltage $V_{GS-S3}$, resonant current $i_L$, output voltage $V_O$, and switch $S_3$ drain-to-source voltage $V_{DS-S3}$ waveforms of experimental circuit for abrupt topology transitions at $V_{IN} = 200$ V and $P_D = 800$ W.

Fig. 14. Measured switch $S_3$ gate-to-source voltage $V_{GS-S3}$, resonant current $i_L$, output voltage $V_O$, and switch $S_3$ drain-to-source voltage $V_{DS-S3}$ waveforms of experimental circuit for 80-ms topology transitions at $V_{IN} = 240$ V and $P_D = 800$ W.
to the FB topology. As it can be seen from Fig. 18, even when the topology transition is interrupted and the circuit is forced to return to the original topology, the output voltage transient is limited to 300 mV, i.e., to less than 0.7%.

Finally, Fig. 19 shows the key waveforms during the output voltage transitions between 48-V and 24-V level. These transitions, with a transition time of 300 ms, are performed at constant input voltage $V_{in}$ = 200 V and constant output power $P_o$ = 400 W by changing (ramping up and down) the output reference voltage during the topology transition periods. As can be seen from Fig. 19, the output voltage for both ramp down and up transitions changes monotonically without any overshoots and/or undershoots.

VII. SUMMARY

In this paper, a control method for on-the-fly topology change, i.e., topology morphing, employed to optimize efficiency of the LLC resonant converter operating with a wide input-voltage and/or output-voltage range is described.

![Fig. 15. Measured switch $S_3$ gate-to-source voltage $V_{GS-S3}$, resonant current $i_L$, output voltage $V_O$, and switch $S_3$ drain-to-source voltage $V_{DS-S3}$ waveforms of experimental circuit for 500-ms topology transitions at $V_{in} = 240$ V and $P_o = 800$ W.](image)

![Fig. 16. Zoomed-in waveforms of Fig. 14 for FB-to-HB transition for duty cycle $D_{S3}$=50, 55, 75, and 100%.](image)
In the proposed approach, the LLC topology is gradually changed between the full bridge (FB) and half bridge (HB) so that a tight output control and uninterrupted power flow are maintained during the transitions. As a result, the output voltage does not exhibit any significant transients during the topology-transition periods.

By changing of power converter’s topology to that which is optimal for given input-voltage and/or output-voltage conditions, converter’s efficiency can be improved. The full-bridge topology is employed when the ratio of the input voltage to the output voltage is in the high range, i.e., when the input voltage is low and/or the output voltage is high, whereas the topology is changed to the half bridge when the input to the output voltage ratio is in the low range, i.e., when the input voltage is high and/or the output voltage is low.

The transition between the two topologies is implemented by pulse-width modulation of the two switches in one of the bridge legs. Specifically, when transitioning from the full-bridge to the half-bridge topology, the duty ratio of one switch is increased from 50% to 100%, while simultaneously the duty ratio of the other switch is reduced from 50% to 0% so that after the transition, one switch is continuously turned on while the other is continuously turned off. The transition from the half-bridge to the full-bridge topology is accomplished by commencing the modulation of the non-switching leg and changing the duty ratios of the switches until they both operate with 50% duty ratio.

The performance of the proposed on-the-fly topology-morphing control is experimentally verified on a 48-V, 800-W, LLC dc/dc converter prototype designed for a 100-V to 400-V input-voltage range. The measured results show that the output voltage stays tightly regulated during topology transitions, exhibiting transients that are below 1% for a transition time as short as 80 ms.
Fig. 19. Measured waveforms for output voltages transitions between 48-V and 24-V level at $V_{in} = 240$ V and constant output power $P_o = 400$ W. It should be noted that because the converter’s output current is limited to $I_o = 16.6$ A, the maximum output power for $V_o = 24$ V is limited to $P_o = 400$ W.

REFERENCES


Milan M. Jovanović (S’85–M’88–SM’89–F’01) was born in Belgrade, Serbia. He received the Dipl. Ing. degree in electrical engineering from the University of Belgrade in 1976. He is currently the Senior Vice President for R&D of Delta Products Corporation, the U.S. subsidiary of Delta Electronics, Inc., Taiwan, one of the world’s largest manufacturers of power supplies.

Brian T. Irving was born in Ossining, New York. He received the Bachelor of Science degree in electrical engineering from the State University of N.Y. at Binghamton, U.S.A.

From 1998-present he has been a Member of R&D Staff at the Delta Power Electronics Laboratory (DPEL). His research interests include low-harmonic rectification, control techniques, current sharing, modeling, and simulation.