

# Single-Stage Single-Switch Input-Current-Shaping Technique with Reduced Switching Loss

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**Abstract**—In this paper, a new single-stage, single-switch input-current-shaping ( $S^4$ ICS) technique which features substantially reduced turn-on switching loss of the switch in a  $S^4$ ICS flyback topology is described. In the proposed technique, the turn-on switching loss due to the discharging of the output capacitance of the switch is reduced by turning on the switch when its voltage is minimum. To achieve the turn-on loss reduction for a wide range of line and load conditions, the flyback transformer is continuously operated at the boundary of the continuous conduction mode (CCM) and discontinuous conduction mode (DCM) by employing a variable-frequency control. The performance of the new  $S^4$ ICS flyback technique was evaluated on a 70-W (20-V/3.5-A) experimental prototype.

**Index Terms**—Line current, power factor correction, single-state ac-dc conversion.

## I. INTRODUCTION

RECENTLY, a number of single-stage input-current-shaping techniques have been introduced. In a single-stage approach, input-current shaping, isolation, and high-bandwidth control are performed in a single step, i.e., without creating a regulated intermediate dc bus. Among the single-stage circuits, a number of circuits described in [1]–[10] seem particularly attractive because they can be implemented with only one semiconductor switch and a simple control. All these single-stage, single-switch input-current shaping ( $S^4$ ICS) circuits integrate the boost-converter front end with the forward-converter or the flyback-converter dc/dc stage. Fig. 1 shows the  $S^4$ ICS flyback converter implementation introduced in [7]. The two additional primary windings,  $N_1$  and  $N_2$ , are employed to keep the voltage of energy-storage (bulk) capacitor  $C_B$  below a desired level in the entire line and load ranges (e.g., 400 V at the universal line range of 90–264 V<sub>rms</sub>). Boost inductor  $L_B$  can operate either in the discontinuous conduction mode (DCM) or in the continuous conduction mode (CCM). Generally, the CCM operation offers a slightly higher efficiency compared to the DCM operation. However, the DCM operation gives a lower total harmonic distortion (THD) of the line current compared to that of the CCM operation.

One of the major contributors to losses of the  $S^4$ ICS flyback converter in Fig. 1 is the turn-on switching loss of switch SW due to the discharging of the output capacitance ( $C_{oss}$ ) of the switch. When the circuit in Fig. 1 operates at a constant switching frequency  $f_s$  with a CCM magnetizing current of the

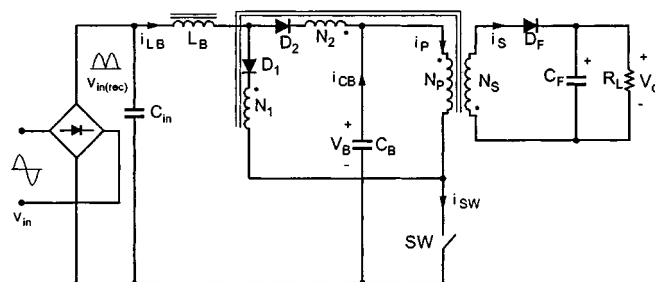


Fig. 1.  $S^4$ ICS flyback converter introduced in [7].

flyback transformer, the power dissipation of the switch associated with the capacitive-discharging turn-on loss is

$$P_{ON(cap)} = C_{oss} V_{SW(off)}^2 f_s / 2, \quad (1)$$

where  $V_{SW(off)} = V_B + nV_o$  is the voltage across the switch during the off-time, and  $n = N_p/N_s$  is the turns ratio of the transformer. Since  $V_{SW(off)}$  increases as the line voltage increases because  $V_B$  increases with the line voltage, the capacitive-discharging turn-on switching loss is maximum at high line. Generally, MOSFET switches with a lower on-resistance,  $R_{DS(on)}$ , which reduces the conduction loss, possess larger output capacitance  $C_{oss}$ . Therefore, at high switching frequencies, the capacitive-discharging turn-on switching loss has a detrimental effect on the efficiency of the circuit in Fig. 1, especially, at high line. Because  $P_{ON(cap)}$  does not depend on the load current but only on the line voltage,  $P_{ON(cap)}$  dominates the switch losses at light loads and, consequently, limits the light-load efficiency. A reduced light-load efficiency makes very difficult to comply with Environmental Protection Agency's Energy Star and similar European requirements, which set a voluntary power-consumption limit of an idling personal computer.

When the flyback transformer in Fig. 1 operates with a DCM magnetizing current, the switch voltage during the off-time after the magnetizing current decreases to zero oscillates around  $V_B$  with an amplitude equal to  $nV_o$  because of the resonance between the magnetizing inductance of the transformer and the output capacitance of the switch. Therefore, the  $S^4$ ICS flyback converter operating with a DCM magnetizing current of the transformer also suffers from capacitive-discharging turn-on switching loss  $P_{ON(cap)}$ . The maximum  $P_{ON(cap)}$  in a DCM flyback converter is the same as the  $P_{ON(cap)}$  in a CCM flyback converter.

In this paper, a new  $S^4$ ICS technique which features substantially reduced turn-on switching loss of the switch in a  $S^4$ ICS flyback converter is described. In this technique, the turn-on switching loss due to the discharging of the output

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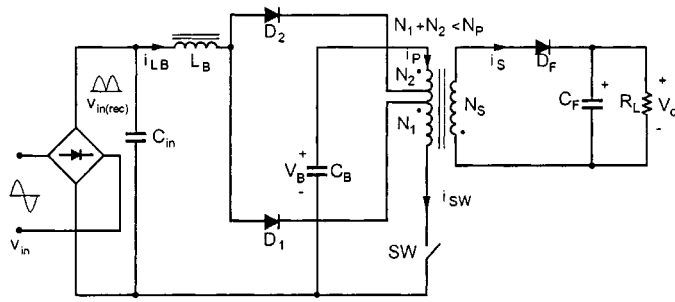


Fig. 2. Implementation of  $S^4ICS$  flyback converter in Fig. 1 with double-tapped primary winding of the transformer.

capacitance of the switch is reduced by turning on the switch when its voltage is minimum or close to the minimum. To achieve the turn-on loss reduction for a wide range of line and load conditions, the flyback transformer is continuously operated at the boundary of the CCM and DCM by employing a variable-frequency control. The implementation of the new  $S^4ICS$  flyback converter is described in Section II, whereas principles of operation, including topological stages and key waveforms, are provided in Section III. Finally, experimental results obtained on a 70-W (20-V/3.5-A) prototype circuit for an adapter application are given in Section IV.

## II. TOPOLOGY

In the  $S^4ICS$  flyback converter in Fig. 1, two additional primary windings,  $N_1$  and  $N_2$ , are employed to keep the voltage of energy-storage (bulk) capacitor  $C_B$  below the desired level in the entire line and load ranges. Winding  $N_1$  appears in series with boost inductor  $L_B$  during the on-time of switch  $SW$ , whereas winding  $N_2$  appears in series with  $L_B$  during the off-time of the switch. By connecting the windings so that the voltage across each of them when they conduct the boost-inductor current is in opposition to the line voltage, the volt-second balance of the boost-inductor core is achieved at a substantially lower voltage of the energy-storage capacitor compared to the corresponding circuit without the windings. In addition, winding  $N_2$  provides a path for a direct transfer of a part of the input energy to the output during the off-time of the switch. Generally, direct energy transfer improves the conversion efficiency.

The same performance of the  $S^4ICS$  converter can be achieved if windings  $N_1$  and  $N_2$  are implemented as portions of the primary winding of the transformer by employing tapping, as shown in Fig. 2. Both implementations of windings  $N_1$  and  $N_2$  require the same number of pins of the transformer. However, since the implementation in Fig. 2 does not require additional windings, the construction of the transformer in Fig. 2 is simpler than that in Fig. 1. The construction of the transformer can be further simplified by selecting  $N_1 + N_2 = N_P$ , because then only one tap on the primary winding is required, as shown in Fig. 3. Also, the  $S^4ICS$  flyback converter in Fig. 3 requires only one diode,  $D$ , instead of two diodes,  $D_1$  and  $D_2$ , in Fig. 2.

Boost inductor  $L_B$  in the  $S^4ICS$  flyback converter in Fig. 1 can operate in both DCM and CCM. For the CCM operation of  $L_B$ , it is necessary to have a substantial inductance connected

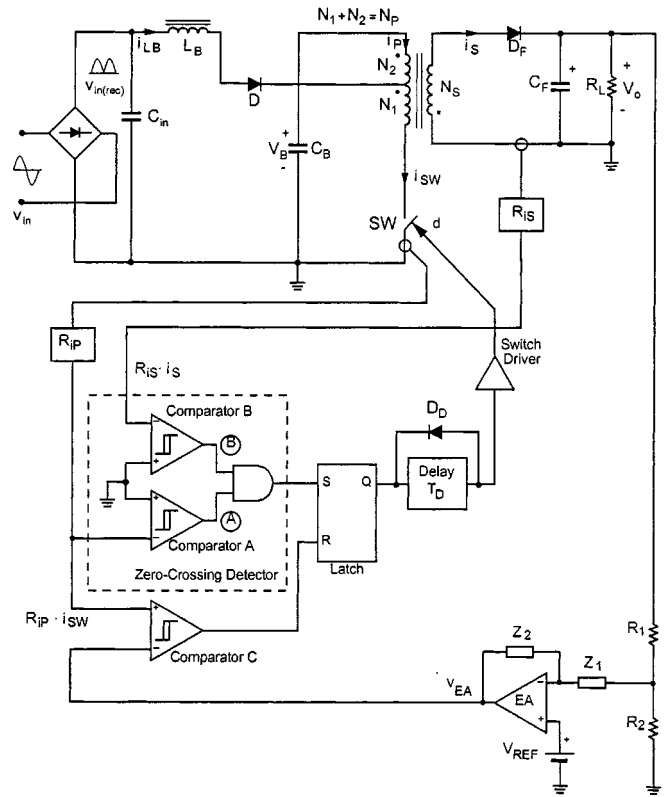


Fig. 3. Power stage and control circuit of the proposed  $S^4ICS$  flyback converter with single-tapped primary winding of the transformer.

in series with winding  $N_1$  and/or winding  $N_2$ , as explained in [8]. The additional inductance can either be the leakage inductance of the winding (implemented by an appropriate structure of the transformer) and/or an external inductance. In the  $S^4ICS$  flyback converter in Fig. 2, boost inductor  $L_B$  can operate also in both DCM and CCM. To achieve the CCM operation of  $L_B$  in Fig. 2, it is more convenient to employ an external inductance in series with diode  $D_1$  and/or diode  $D_2$ . It should be noticed that the  $S^4ICS$  flyback converter in Fig. 3 is only suitable for the DCM operation of  $L_B$ .

## III. PRINCIPLES OF OPERATION

Principles of operation are illustrated on the example of the  $S^4ICS$  flyback converter in Fig. 3. To facilitate the analysis of operation, Figs. 4 and 5 show topological stages and key waveforms of the variable-frequency  $S^4ICS$  flyback converter in Fig. 3, respectively. To simplify the analysis, it is assumed that all semiconductor components are ideal except for the output capacitance of the primary switch,  $C_{oss}$ . In addition, the flyback transformer is modeled by an ideal transformer with magnetizing inductance  $L_M$  in parallel with primary winding  $N_P$ , as shown in Fig. 4. Finally, the input voltage of the converter is considered constant during a switching cycle because the switching frequency is much larger than the line frequency.

Since boost inductor  $L_B$  in Fig. 3 operates in the DCM and the magnetizing inductance of the flyback transformer operates at the DCM/CCM boundary, at the moment immediately before switch  $SW$  is turned on, currents  $i_{LB}$ ,  $i_M$ , and  $i_S$  are zero. After switch  $SW$  is closed at  $t = T_0$ ,  $i_M$  starts flowing through the

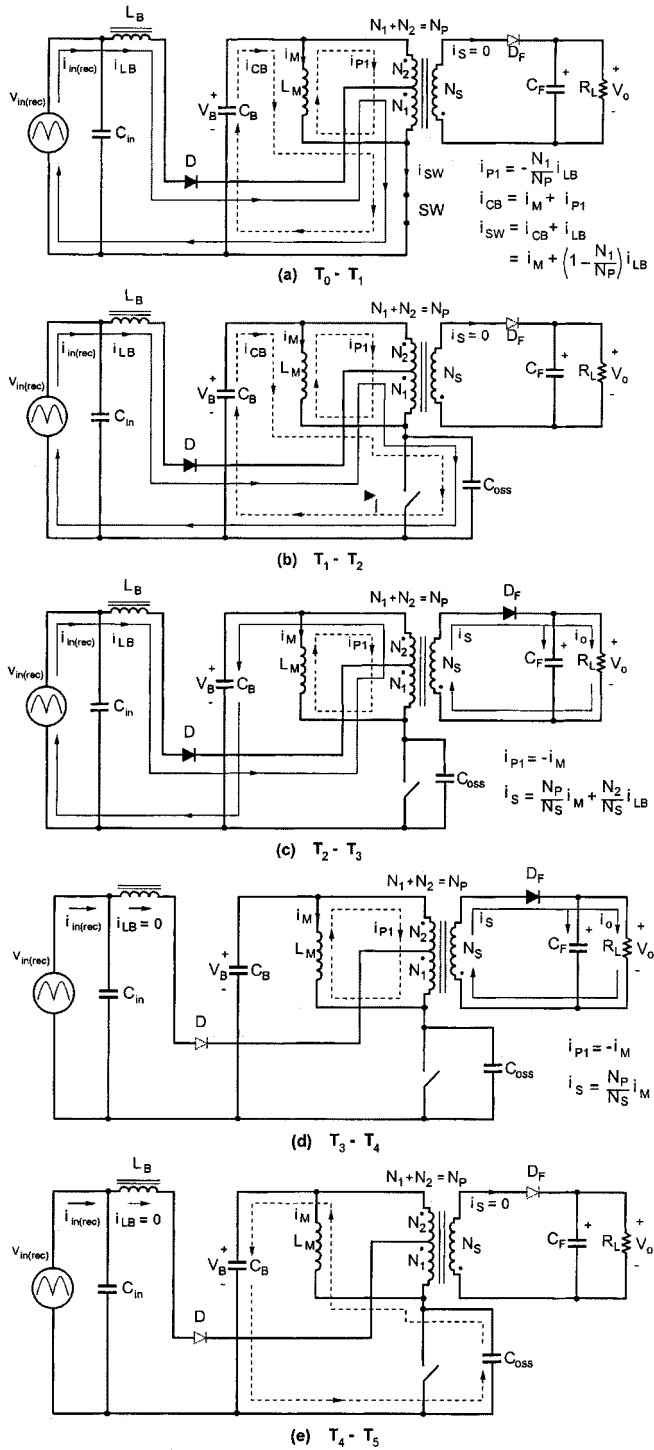


Fig. 4. Topological stages of the  $S^4ICS$  flyback converter in Fig. 3.

switch, as shown in Fig. 4(a). Since energy-storage capacitor voltage  $V_B$  is approximately constant during a switching cycle, magnetizing current  $i_M$  increases linearly with a slope

$$\frac{di_M}{dt} = \frac{V_B}{L_M} \quad (2)$$

as shown in Fig. 5. If rectified line voltage  $v_{in(rec)}$  is lower than  $(N_1/N_P)V_B$ , no boost-inductor current  $i_{LB}$  can flow because

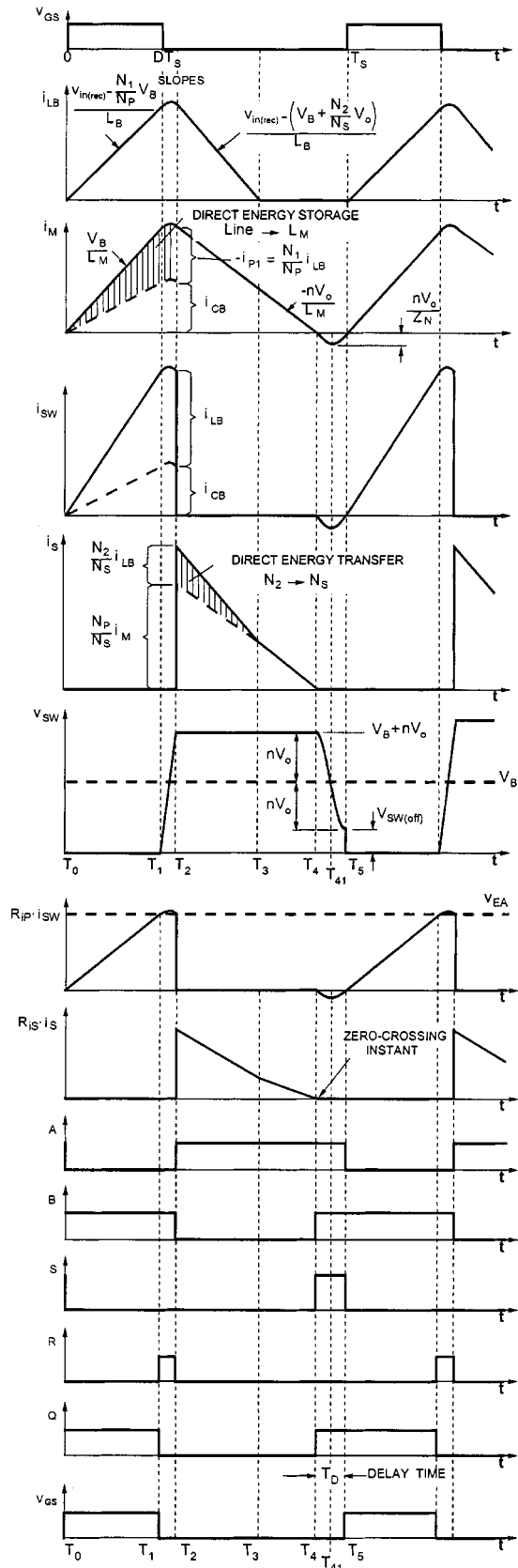


Fig. 5. Key waveforms of the  $S^4ICS$  flyback converter in Fig. 3.

diode  $D$  is reverse biased. Otherwise,  $i_{LB}$  flows through diode  $D$ , winding  $N_1$ , and switch  $SW$  as indicated in Fig. 4(a). The

slope of  $i_{LB}$  is given by

$$\frac{di_{LB}}{dt} = \frac{v_{in(rec)} - (N_1/N_P)V_B}{L_B}. \quad (3)$$

Because of the magnetic coupling between windings  $N_1$  and  $N_2$ , current  $i_{P1}$  flowing through both  $N_1$  and  $N_2$  is

$$i_{P1} = -\frac{N_1}{N_P}i_{LB}. \quad (4)$$

Also, as can be seen from Fig. 4(a), energy-storage-capacitor current  $i_{CB}$  is

$$i_{CB} = i_M + i_{P1} = i_M - \frac{N_1}{N_P}i_{LB}. \quad (5)$$

By rewriting (5) as

$$i_M = i_{CB} + \frac{N_1}{N_P}i_{LB} \quad (6)$$

it can be seen that during the on-time, energy from two sources is stored in the magnetic field of the flyback transformer. Namely, part of the magnetizing energy is supplied from the bulk capacitor, as in the case of the conventional flyback converter, whereas part of the energy is supplied directly from the line. Generally, direct energy storage from the line improves the conversion efficiency. The two components of  $i_M$  are indicated in the  $i_M$  waveform in Fig. 5.

Finally, the switch current is obtained as

$$i_{SW} = i_{CB} + i_{LB} = i_M + \left(1 - \frac{N_1}{N_P}\right)i_{LB}. \quad (7)$$

As can be seen in Fig. 3, during the on-time, the output of comparator  $A$  in the zero-crossing-detector circuit is low, whereas the output of comparator  $B$  is high. Consequently, the output of the AND gate is low, holding the set ( $S$ ) input of the  $SR$  latch low during the entire on-time.

The on-time of the switch is terminated at  $t = T_1$  when sensed voltage  $R_{iP}i_{SW}$  at the input of comparator  $C$  reaches the level of control voltage  $v_{EA}$ . At that moment the reset ( $R$ ) input of the latch changes from low level to high level, forcing the latch output  $Q$  to change from high to low. Because diode  $D_D$  is connected in parallel to the delay circuit, the high-to-low transition of  $Q$  is immediately transferred to the input of the switch driver, i.e., switch  $SW$  is turned off without a delay.

After switch  $SW$  is turned off, currents  $i_{LB}$  and  $i_{CB}$  continue to flow through output capacitance  $C_{oss}$  of the switch, as shown in Fig. 4(b), and switch voltage  $v_{SW}$  starts increasing. When switch voltage  $v_{SW}$  reaches  $V_B + nV_o$  at  $t = T_2$ , secondary-side rectifier  $D_F$  becomes forward biased, as shown in Fig. 4(c). Because of the conduction of rectifier  $D_F$ , switch voltage  $v_{SW}$  stays clamped to  $V_B + nV_o$ . At the same time, reflected magnetizing current  $(N_P/N_S)i_M = -((N_P/N_S)i_{P1})$  starts flowing on the secondary side. In addition, at  $t = T_2$ , boost-inductor current  $i_{LB}$  begins flowing through diode  $D$ , winding  $N_2$ , and energy-storage capacitor  $C_B$ , as shown in Fig. 4(c). Because of the magnetic coupling between winding  $N_2$  and secondary

winding  $N_S$ ,  $i_{LB}$  is also reflected to the secondary. According to Fig. 4(c), the secondary current is given by

$$i_S = \frac{N_P}{N_S}i_M + \frac{N_2}{N_S}i_{LB}. \quad (8)$$

As can be seen from (8),  $i_S$ , which during the off-time supplies energy to the output, is composed of two components which draw energy from two different sources. The energy of the component associated with the magnetizing current is obtained from the energy stored in the magnetic field during the on-time, while the energy associated with the boost-inductor current is drawn directly from the input line. The two  $i_S$  components are indicated in the  $i_{LB}$  waveform in Fig. 5. Generally, direct energy transfer from the line to the output improves the conversion efficiency.

It should be noticed that at  $t = T_2$  the outputs of comparators  $A$  and  $B$  in the zero-crossing-detector circuit in Fig. 3 change states. Namely, the output of comparator  $A$  changes from low to high, whereas the output of comparator  $B$  changes from high to low. These changes do not have any effect on the output of the AND gate, i.e., the  $S$  input of the latch, which continues to stay low. However, at  $t = T_2$ , the  $R$  input of the latch changes state from high to low because the primary current stops flowing and sensed voltage  $R_{iP}i_{SW}$  becomes zero. Since the  $SR$  latch is only triggered with positive edge transitions, the high-to-low transition at the  $R$  input does not change the state of the latch, i.e., output  $Q$  stays low keeping switch  $SW$  off.

It should be also noticed that at  $t = T_2$ , the instantaneous, simultaneous transitions of the outputs of comparators  $A$  and  $B$  in the opposite directions create a signal-racing situation. This may generate a false pulse at the AND-gate output that may false trigger the latch. This racing situation in Fig. 5 is the result of the assumption that the leakage inductances of the transformer are negligible so that switch current  $i_{SW}$  and secondary current  $i_S$  commute instantaneously. However, in a practical circuit, due to the leakage inductances of the transformer, the commutation of the currents takes a short but finite time. In fact, in the presence of the leakage inductances, the output of comparator  $B$  changes from high to low at  $t = T_2$ , which marks the beginning of the commutation period, whereas the output of comparator  $A$  changes state at the end of the commutation period, which occurs at a later instant. Therefore, in the presence of the leakage inductances of the transformer, the signal racing at  $t = T_2$  does not exist, and no false triggering of the latch can occur.

As can be seen from Fig. 5, after  $t = T_2$ , currents  $i_{LB}$  and  $i_M$  decrease linearly. According to Fig. 4(c), the downslope of  $i_{LB}$  is given by

$$\frac{di_{LB}}{dt} = -\frac{V_B + (N_2/N_S)V_o - v_{in(rec)}}{L_B} \quad (9)$$

whereas the downslope of  $i_M$  is given by

$$\frac{di_M}{dt} = -\frac{nV_o}{L_M}. \quad (10)$$

From (9), it can be seen that winding  $N_2$  reduces energy-storage-capacitor voltage  $V_B$  required to reset  $L_B$  for the amount of the induced voltage  $(N_2/N_S)V_o$  across winding  $N_2$ .

When at  $t = T_3$ ,  $i_{LB}$  decreases to zero, diode  $D$  turns off, as shown in Fig. 4(d). However, the linearly decreasing magnetizing current  $(N_P/N_S)i_M = -(N_P/N_S)i_{P1}$  continues to flow in the secondary until it becomes zero at  $t = T_4$  (Fig. 5).

To operate the flyback converter at the DCM/CCM boundary, primary switch  $SW$  needs to be turned on immediately after  $i_S$  falls to zero at  $t = T_4$ . However, if switch  $SW$  is turned on at  $t = T_4$ , capacitive-discharging turn-on loss  $P_{ON(cap)}$  would not be reduced because switch  $SW$  would be turned on with voltage  $V_{SW(off)} = V_B + nV_o$  across it. To achieve a reduction of  $P_{ON(cap)}$ , it is necessary to delay the turn-on of primary switch  $SW$  with respect to the instant at which secondary current  $i_S$  falls to zero. This can be achieved by inserting a delay circuit between the output of the  $SR$  latch and the switch driver, as shown in Fig. 3. When  $i_S$  becomes zero at  $t = T_4$ , the output of comparator  $B$  in the zero-crossing detector changes from low to high, causing the output of the AND gate ( $S$  input of the latch) to go high. The low-to-high transition at the  $S$  input of the latch causes the  $Q$  output of the latch to also change from low to high. However, because of the delay circuit, the change at the latch output appears at the input of the switch driver after a constant delay  $T_D$ . This delay is determined so that switch  $SW$  is turned on with the minimum voltage across it.

As shown in Fig. 4(e), when switch  $SW$  is kept off after  $t = T_4$ , magnetizing inductance  $L_M$  of the transformer and output capacitance  $C_{oss}$  of the switch form a series resonant circuit. During the resonance, switch voltage  $v_{SW}$  decreases and reaches a minimum of

$$V_{SW(off),min} = V_B - nV_o. \quad (11)$$

at  $t = T_5$ . Therefore, to turn switch  $SW$  on with a minimum voltage across it, the required delay time of the controller is equal to one-half of a resonant period of the  $L_M - C_{oss}$  resonant circuit, i.e.,

$$T_D = \pi \sqrt{L_M C_{oss}}. \quad (12)$$

However, it should be noted that  $C_{oss}$  is dependent on the voltage (nonlinear capacitance), and that both  $L_M$  and  $C_{oss}$  are temperature dependent. Therefore, the constant delay calculated from (12) does not ensure that switch  $SW$  is turned on at the minimum voltage under all operating conditions. Nevertheless, the switch would be turned on close to the minimum voltage since the variations of the parameters in (12) are not large.

Finally, when switch  $SW$  is turned on at  $t = T_5$  by the delayed transition at the  $S$  input of the  $SR$  latch, the output of comparator  $A$  changes from high to low causing the output of the AND gate ( $S$  input of the latch) to go low.

Since the control circuit in Fig. 3 does not have a clock to initiate a switching transition, but the turn-on and turn-off switching instants are determined by comparisons of sensed primary and secondary currents with the zero reference level, the controller works with a variable switching frequency. Moreover, both the on-time and the off-time are variable. The frequency is maximum at the highest line voltage and the minimum load, whereas the minimum switching frequency occurs at the lowest line voltage and the full load.

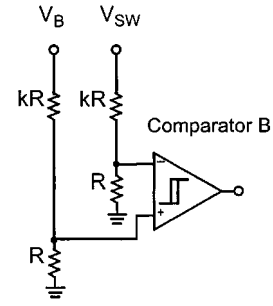


Fig. 6. Implementation of comparator  $B$  by sensing the primary voltage.

Switch  $SW$  can be turned on with zero voltage if the circuit is designed so that  $nV_o \geq V_B$ . To achieve zero-voltage switching (ZVS) in the entire line range, the ZVS condition must be met at the highest line voltage, when  $V_B = V_{B,max}$ , which results in a maximum switch voltage of  $V_{SW,max} \geq 2V_{B,max}$ . In universal-line (90–264 V<sub>rms</sub>) applications, where a typical value of  $V_{B,max}$  is around 400 V, a design which achieves ZVS in the entire line range would require a switch with a voltage rating in excess of 800 V. Since higher voltage-rated switches have higher on-resistance and are more expensive than their counterparts with lower voltage ratings, a design with ZVS in the entire line range neither gives the optimal performance nor it is cost effective. In fact, in a design with the optimum trade-off between performance and cost,  $nV_o$  is selected based on the desirable maximum stress of the switch with a lower voltage (e.g., 600 V) rating. However, for such a selection of  $nV_o$ , no ZVS is achieved at high line and, very often, it is not achieved even at low line. Still, the switch is turned on with a substantially reduced voltage, resulting in a significantly lower capacitive-discharging turn-on switching loss.

The circuit in Fig. 3 can be implemented in a number of different ways. For example, the onset of the DCM can be detected by sensing the primary or secondary voltage of the transformer instead of sensing the secondary current. As an illustration, Fig. 6 shows the implementation of comparator  $B$  in the circuit in Fig. 3 by sensing the primary voltage, i.e., the difference between bulk voltage  $V_B$  and switch voltage  $v_{SW}$  to detect the beginning of the DCM. With this implementation of comparator  $B$ , the onset of the DCM is sensed by detecting the time instant  $t = T_{41}$  in Fig. 5 when switch voltage  $v_{SW}$  falls below  $V_B$ . As can be seen from the  $v_{SW}$  waveform in Fig. 5, to achieve the minimum turn-on loss in this implementation of comparator  $B$ , the delay of the controller needs to be one half of that in Fig. 3, which is given in (12).

Finally, it should be noticed that in some applications, the conversion efficiency of the flyback S<sup>4</sup>ICS can be improved by replacing secondary-side rectifier  $D_F$  in Fig. 3 by a synchronous rectifier, i.e., very low on-resistance MOSFET [11].

#### IV. EXPERIMENTAL RESULTS

To verify the operation and performance of the new S<sup>4</sup>ICS technique, a 70-W (20-V/3.5-A), universal line voltage (90–264 V<sub>rms</sub>) S<sup>4</sup>ICS flyback converter shown in Fig. 3 with comparator  $B$  shown in Fig. 6 was built for an adapter application. The following components were used in the implementation of the

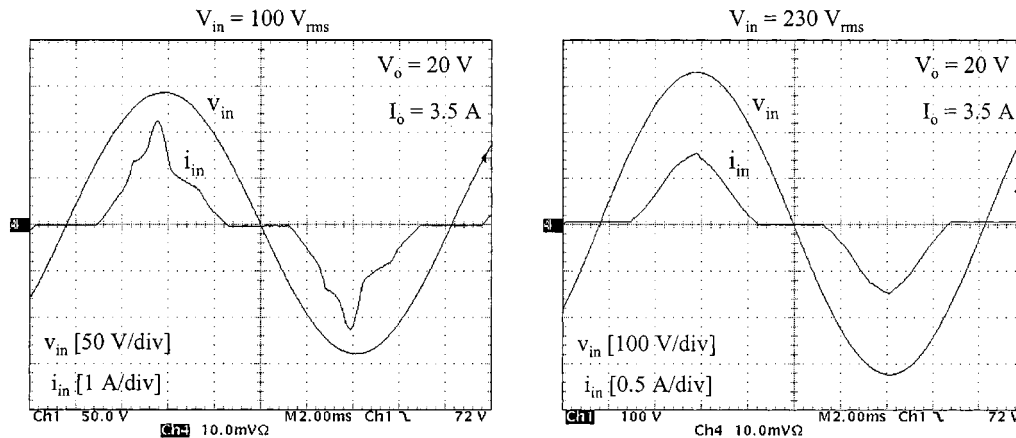


Fig. 7. Experimental line-voltage and line-current waveforms.

TABLE I  
MEASURED PF, THD,  $V_B$ , EFFICIENCY, AND SWITCHING FREQUENCY  
AT FULL LOAD

$V_{in}$ [V <sub>rms</sub> ]	PF	THD [%]	$V_B$ [V]	$\eta$ [%]	$f_s$ [kHz]
90	0.884	51.4	120	84.2	41-71
100	0.886	51.5	134	84.9	45-79
132	0.902	47.0	180	86.9	59-96
180	0.908	45.7	250	87.8	73-106
230	0.903	47.0	325	87.9	85-116
264	0.896	48.6	378	87.7	91-120

circuit:  $C_{in} = 220$  nF/250 Vac,  $L_B = 180$   $\mu$ H,  $D = \text{BYM26C}$ ,  $C_B = 180$   $\mu$ F/400 V, Transformer - EER28L core with  $N_P = 66$  turns,  $N_S = 11$  turns,  $N_1 = N_2 = 33$  turns,  $L_M = 520$   $\mu$ H,  $SW = \text{SPPX1N60S5}$  (600 V, 20 A, 0.19  $\Omega$ ),  $D_F = 16\text{CTQ100}$ ,  $C_F = 3 \times 470$   $\mu$ F/25 V. The control circuit was implemented using the variable-frequency power-factor-controller integrated circuit MC34262. Measured full-load line-voltage and line-current waveforms at the nominal low line ( $V_{in} = 100$  V<sub>rms</sub>) and the nominal high line ( $V_{in} = 230$  V<sub>rms</sub>) are shown in Fig. 7. The measured individual line-current harmonics were well below the IEC1000-3-2 Class-D limits, i.e., they exhibited more than 20% margin at both the nominal low line and high line. Table I summarizes the measured full-load power-factor (PF), total-harmonic-distortion (THD), bulk-capacitor-voltage ( $V_B$ ), efficiency, that includes electromagnetic interference (EMI) filter and in-rush current limiter losses, and switching-frequency range. As can be seen from Table I, the maximum bulk-capacitor voltage is well below 400 V. The minimum efficiency, which occurs at low line, is above 84%.

## V. CONCLUSION

A new single-stage, single-switch input-current-shaping ( $S^4$ ICS) technique which features substantially reduced turn-on switching loss of the switch in a  $S^4$ ICS flyback converter is proposed. The turn-on switching loss due to the discharging of the output capacitance of the switch is reduced by turning on

the switch when its voltage is minimum or close to minimum. To achieve the turn-on loss reduction for a wide range of line and load conditions, the flyback transformer is continuously operated at the boundary of the discontinuous and continuous conduction modes (DCM/CCM) by employing a variable-frequency control. The wide-bandwidth, variable-frequency control is implemented by detecting the onset of the DCM/CCM boundary and, subsequently, turning on the switch with an appropriate delay when the switch voltage becomes minimum. Because of the flyback converter topology, the proposed technique is most suitable for universal-line (90–264 V<sub>rms</sub>) applications with higher output voltages and lower output currents. Due to the DCM/CCM boundary operation, the maximum energy-storage-capacitor voltage in the proposed technique is well below 400 V.

## REFERENCES

- [1] M. Madigan, R. Erickson, and E. Ismail, "Integrated high-quality rectifier-regulators," in *IEEE Power Electron. Specialists Conf. (PESC) Rec.*, June 1992, pp. 1043–1051.
- [2] S. Teramoto, M. Sekine, and R. Saito, "High power factor ac/dc converter," U.S. Patent 5 301 095, Apr. 5, 1994.
- [3] R. Redl and L. Balogh, "Design consideration for single-stage isolated power-factor corrected supplies with fast regulation of the output voltage," in *IEEE Appl. Power Electron. Conf. (APEC) Proc.*, Mar. 1995, pp. 454–458.
- [4] H. Watanabe, Y. Kobayashi, Y. Sekine, M. Morikawa, and T. Ishii, "The suppressing harmonic currents, MS (magnetic switch) power supply," in *Proc. IEEE Int. Telecommun. Energy Conf. (INTELEC)*, Oct. 1995, pp. 783–790.
- [5] F. S. Tsai, P. Markowski, and E. Whitcomb, "Off-line flyback converter with input harmonic current correction," in *Proc. IEEE Int. Telecommun. Energy Conf. (INTELEC)*, Oct. 1996, pp. 120–124.
- [6] J. Qian and F. C. Lee, "A high efficient single stage single switch high power factor ac/dc converter with universal input," in *Proc. IEEE Appl. Power Electron. Conf. (APEC)*, Feb. 1997, pp. 281–287.
- [7] L. Huber and M. M. Jovanović, "Single-stage, single-switch isolated power-supply technique with input-current shaping and fast output-voltage regulation," in *Proc. IEEE Appl. Power Electron. Conf. (APEC)*, Feb. 1997, pp. 272–280.
- [8] —, "Design optimization of single-stage, single-switch input-current shapers," in *IEEE Power Electron. Specialists Conf. (PESC) Rec.*, June 1997, pp. 519–526.
- [9] J. Sebastian, M. M. Hernando, P. Villegas, J. Diaz, and A. Fontan, "Input current shaper based on the series connection of voltage source and a loss-free resistor," in *Proc. IEEE Appl. Power Electron. Conf. (APEC)*, Feb. 1998, pp. 461–467.
- [10] G. Hua, "Consolidated soft-switching ac/dc converters," U.S. Patent 5 790 389, Aug. 4, 1998.

- [11] M. T. Zhang, M. M. Jovanović, and F. C. Lee, "Design considerations and performance evaluations of synchronous rectification in flyback converters," in *Proc. IEEE Appl. Power Electron. Conf. (APEC)*, Feb. 1997, pp. 623–630.



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