

Single-Stage Input-Current-Shaping Technique with Voltage-Doubler-Rectifier Front End

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Abstract—In this paper, a new single-stage input-current-shaping (S²ICS) technique that integrates the voltage-doubler-rectifier front end with a dc/dc output stage is introduced. Due to the voltage-doubler-rectifier front end, a reduction of line-current harmonics can be achieved with a higher conversion efficiency compared to the corresponding S²ICS circuit with the conventional wide-range full-bridge rectifier. The proposed technique requires energy-storage capacitors with the same total capacitance and with half of the voltage rating as in the conventional S²ICS counterpart, which reduces the size and cost of the power supply. The performance of the proposed technique is evaluated on a 450-W (5-V/90-A) experimental prototype circuit.

Index Terms—Line current shaper, power factor correction, single-stage ac-dc conversion, voltage-doubler rectifier.

I. INTRODUCTION

A number of single-stage input-current-shaping (S²ICS) techniques have been introduced recently. In a single-stage approach, input current shaping (ICS), isolation, and high-bandwidth control are performed in a single step, i.e., without creating a regulated intermediate dc bus. Generally, S²ICS circuits meet European and/or Japanese regulatory requirements regarding line current harmonics, but they do not improve the power factor (PF) and reduce the total harmonic distortion (THD) as much as their conventional two-stage counterparts. Typically, PF for S²ICS circuits is between 0.8 and 0.9, whereas their THD is in the 40–75% range.

Among the single-stage circuits, a number of circuits described in [1]–[12] seem particularly attractive because they can be implemented with only one semiconductor switch and a simple control. All these S²ICS circuits integrate a boost ICS stage with a forward or flyback dc/dc-converter stage.

Although it has been demonstrated that the S²ICS circuits described in [1]–[12] can achieve the desired performance in a variety of applications, the S²ICS power supplies have significant difficulties meeting performance expectations in universal-line (90–270-Vac) applications with a hold-up time requirement. For example, most of today's desktop computers and computer peripherals require power supplies that are capable of operating in the 90–270-Vac range and can provide a hold-up time of at least 10 ms. Generally, the hold-up time is the time during which a

power supply must maintain its output voltage(s) within a specified range after a drop-out of the line voltage. The hold-up time is used to orderly terminate the operation of a computer or to switch over to an uninterruptible-power-supply (UPS) operation after a line failure. The required energy to support the output during the hold-up time is obtained from a properly sized energy-storage capacitor, C_B , which is used to handle the differences between a varying instantaneous input power and a constant output power. The difficulty of these S²ICS circuits to deal with a wide line range and long hold-up time requirement stems from the fact that the voltage of the energy-storage capacitor, V_B , varies with the line voltage and load current [4]. In most applications, with a proper design, V_B can be kept in the 410–420 Vdc range, which warrants the use of a 450-V electrolytic capacitor. Since the value of C_B is determined from the hold-up time requirement at the minimum line (worst case), the S²ICS approach requires a relatively bulky and expensive energy-storage capacitor. Moreover, due to a wide-range variation of V_B , which is the input to the dc/dc output stage, the conversion efficiency of the dc/dc output stage is reduced. In contrast, the two-stage approach, in which V_B is independently regulated at approximately 380 Vdc, requires a much smaller and, therefore, cheaper electrolytic capacitor rated at 450 V, or even 400 V. In addition, due to a regulated V_B , the efficiency of the dc/dc output stage in the two-stage approach can be made higher compared to that in the single-stage approach.

Generally, the performance of conventional, universal-line-range power supplies without ICS can be improved by employing a voltage-doubler rectifier (VDR) [13]. The output voltage of a VDR front end is approximately the same for both the low-line range (90–135 Vac) and the high-line range (180–270 Vac), i.e., it varies from approximately $\sqrt{2} \cdot 180$ Vdc to $\sqrt{2} \cdot 270$ Vdc. Since this voltage range is half of the corresponding voltage range of the conventional wide-range full-bridge rectifier (FBR), the conversion efficiency of the dc/dc output stage can be improved. In addition, because the minimum voltage of the VDR is twice as high as that of the wide-range FBR, the total capacitance required for a given hold-up-time specification is approximately the same as the capacitance required in the wide-range FBR. However, the capacitors in the VDR need to be rated at only 250 Vdc, or even 200 Vdc. Usually, electrolytic capacitors with a lower voltage rating are significantly cheaper than their counterparts with a higher voltage rating.

In this paper, a new S²ICS technique that integrates the voltage-doubler-rectifier front end with a dc/dc output stage is introduced. First, in Section II, the S²ICS technique with the conventional wide-range FBR is reviewed. The S²ICS converters with the wide-range FBR can be classified in two

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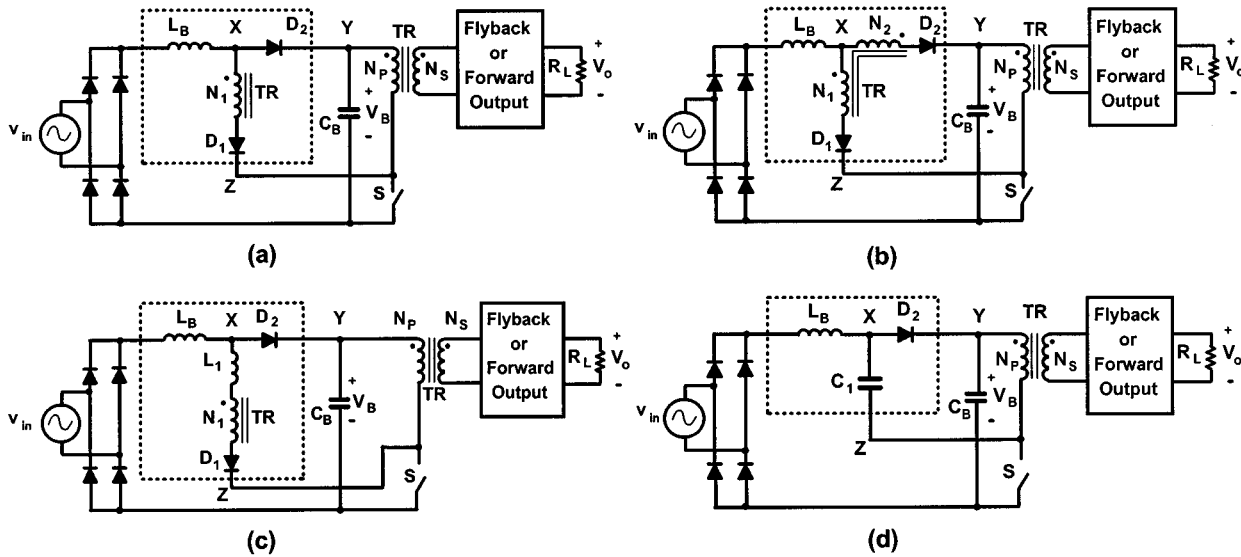


Fig. 1. S^2 ICS circuits with three-terminal ICS cells: (a) DCM ICS cell with winding N_1 [7], (b) DCM ICS cell with windings N_1 and N_2 [8], (c) inductive CCM ICS cell [11], [12], and (d) capacitive CCM ICS cell [3].

families: the S^2 ICS family with two-terminal ICS cells and the S^2 ICS family with three-terminal ICS cells. In this paper, these two S^2 ICS families were also extended to the voltage-doubler S^2 ICS (VDS 2 ICS) converter implementations: the VDS 2 ICS family with two-terminal ICS cells and the VDS 2 ICS family with three-terminal ICS cells. In Section III, generalized circuit diagrams and principles of operation for both the VDS 2 ICS family with two-terminal ICS cells and the VDS 2 ICS family with three-terminal ICS cells are presented. Finally, experimental results obtained on a 450-W (5-V/90-A) prototype circuit are given in Section IV.

II. REVIEW OF S^2 ICS CONVERTERS WITH WIDE-RANGE FBR

Generally, the S^2 ICS converters can be classified in two families: the S^2 ICS family with two-terminal ICS cells and the S^2 ICS family with three-terminal ICS cells. Although topologically different, the two S^2 ICS families are functionally equivalent and exhibit very similar performance.

The ICS inductor of a S^2 ICS circuit with two-terminal or three-terminal ICS cells can operate either in the discontinuous conduction mode (DCM) or in the continuous conduction mode (CCM). In the DCM operation of the ICS inductor, low line-current harmonic distortions are achieved because of the inherent property of the DCM boost converter to draw a near sinusoidal current if its duty cycle is held relatively constant during a half line cycle. Generally, the DCM operation gives a lower THD of the line current compared to the CCM operation. However, the CCM operation yields a slightly higher efficiency compared to the DCM operation.

A. S^2 ICS Family with Three-Terminal ICS Cells

A typical S^2 ICS circuit with DCM operation of the ICS inductor is shown in Fig. 1(a) [7]. The ICS cell, shown in the dotted rectangle in Fig. 1(a), consists of ICS inductor L_B and two current paths: path XZ for charging L_B when switch S is

on and path XY for discharging L_B when switch S is off. Since charging path XZ is connected to switch S and discharging path XY is connected to energy-storage capacitor C_B , the ICS cell in Fig. 1(a) has three terminals. The function of the transformer winding N_1 in path XZ is to limit the voltage on energy-storage capacitor C_B and to improve the overall efficiency. However, winding N_1 also introduces line-current distortions around the zero crossings because the line current cannot flow when the instantaneous line voltage is lower than the voltage induced across winding N_1 . Therefore, in the S^2 ICS circuit in Fig. 1(a) there is a strong trade-off between PF, THD, and efficiency. To further reduce the energy-storage capacitor voltage and improve efficiency, another transformer winding, N_2 , can be placed in discharging path XY as shown in Fig. 1(b) [8]. During the discharging of the ICS inductor, the voltage across windings N_2 has the same direction as the voltage across the energy-storage capacitor, i.e., winding N_2 effectively increases the reset voltage across the ICS inductor. As a result, the required reset voltage for L_B can be obtained with a lower voltage on energy-storage capacitor C_B . It should be noted that since windings N_1 and N_2 are magnetically coupled to the secondary winding of transformer TR , they can be used to directly transfer energy from the input (line) to the load. Winding N_1 provides direct energy transfer with the forward-type dc/dc power stages, while winding N_2 provides direct energy transfer with the flyback-type dc/dc power stages. Generally, direct energy transfer improves the conversion efficiency.

To achieve CCM operation of the ICS inductor, an additional inductor or capacitor is required as shown in Fig. 1(c) [11], [12] and Fig. 1(d) [3], respectively. The function of inductor L_1 in Fig. 1(c) and capacitor C_1 in Fig. 1(d) is to provide a variable effective duty cycle for boost inductor L_B even when the duty cycle of switch S is relatively constant during a half line cycle. Namely, to achieve a good tracking of the line current and line voltage with boost inductor L_B operating in CCM, it is necessary that the duty cycle of L_B , D_{LB} , defined as the ratio of the

charging time of L_B and the switching period, is proportional to the instantaneous line voltage during a half line cycle. Specifically, D_{LB} should be maximum around the zero crossings of the line voltage and minimum around the line voltage peaks, i.e.,

$$D_{LB} \approx 1 - |v_{in}|/V_B. \quad (1)$$

Inductor L_1 in Fig. 1(c) modulates boost-inductor duty cycle D_{LB} by delaying the commutation of the boost inductor current from path XY to path XZ after switch S is turned on. Since during this commutation time, which is proportional to the line current and, therefore, to the line voltage, L_B continues to discharge, duty cycle D_{LB} varies with the line voltage even though the duty cycle of switch S is relatively constant. Similarly, in Fig. 1(d), capacitor C_1 modulates D_{LB} by speeding up the commutation of the boost-inductor current from path XZ to path XY after switch S is turned on. Namely, after switch S is turned on, boost-inductor current charges capacitor C_1 until C_1 is charged to V_B . Once C_1 is charged to V_B , the boost-inductor current commutates to path XY . As a result, duty cycle D_{LB} is different from the duty cycle of switch S . Furthermore, since the charging time of C_1 is proportional to the boost-inductor current, D_{LB} varies with the line voltage as shown in (1).

In all S^2 ICS circuits in Fig. 1, the three-terminal ICS cell, shown in the dotted rectangle, has the same basic topology that includes ICS inductor L_B connected to the output of the full-bridge rectifier, L_B charging path XZ connected to switch S , and L_B discharging path XY connected to energy-storage capacitor C_B . Therefore, all S^2 ICS circuits in Fig. 1 can be represented by a S^2 ICS circuit with a generalized three-terminal ICS cell as shown in Fig. 2. The generalized three-terminal ICS cell in Fig. 2 consists of ICS inductor L_B , the boost inductor charging path P_{ch} between nodes X and Z , and the boost inductor discharging path P_{dch} between nodes X and Y . The L_B charging and discharging paths each includes at least one of the following components: a diode, a transformer winding, an inductor, and a capacitor.

Finally, it should be noted that windings N_1 and N_2 in Fig. 1 can be implemented by tapping the primary winding of the power transformer [11], [12]. While tapping simplifies the transformer design, it has no effect on the operation of the S^2 ICS circuits.

B. S^2 ICS Family with Two-Terminal ICS Cells

Another implementation of the DCM S^2 ICS circuit is shown in Fig. 3(a) [6]. In this implementation, a two-terminal ICS cell, shown in the dotted rectangle, is inserted between the full-bridge rectifier and the energy-storage capacitor. The two-terminal ICS cell in Fig. 3(a) consists of ICS inductor L_B , the charging path of L_B (the path with D_1 and N_1^*), and the discharging path of L_B (the path with D_2). The charging and discharging paths of L_B are connected in parallel. The polarity of transformer winding N_1^* is such that the voltage across it is in opposition to the bulk voltage V_B during the on-time of switch S , therefore, decreasing the voltage at node X . To obtain the same voltage at node X during the on-time of switch S as in the corresponding

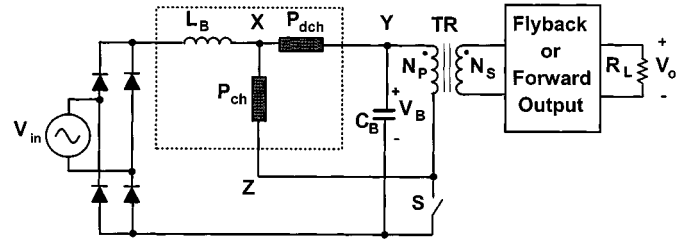


Fig. 2. S^2 ICS circuit with generalized three-terminal ICS cell.

three-terminal cell in Fig. 1(a), the number of turns of winding N_1^* should be

$$N_1^* = N_P - N_1 \quad (2)$$

where N_1 is the number of turns of winding N_1 in Fig. 1(a). The discharging path of L_B in the two-terminal ICS cell in Fig. 3(a) is identical to the discharging path of L_B in the corresponding three-terminal ICS cell in Fig. 1(a). Therefore, with $N_1^* = N_P - N_1$, the S^2 ICS circuit with the two-terminal ICS cell in Fig. 3(a) is functionally equivalent to the S^2 ICS circuit with the three-terminal ICS cell in Fig. 1(a).

Generally, for each S^2 ICS circuit with a three-terminal ICS cell in Fig. 1, there exists a functionally equivalent S^2 ICS circuit with a two-terminal ICS cell. The corresponding S^2 ICS circuit with a two-terminal ICS cell to the S^2 ICS circuit with the three-terminal ICS cell in Fig. 1(b) is presented in Fig. 3(b). For the S^2 ICS circuits with the three-terminal CCM ICS cells in Fig. 1(c) and (d), the corresponding S^2 ICS circuits with two-terminal ICS cells are shown in Fig. 3(c) [10] and Fig. 3(d) [5], respectively. Finally, the S^2 ICS circuit with the generalized two-terminal ICS cell is shown in Fig. 4. It should be noted that the two-terminal ICS cell in Fig. 3(b) can be simplified for the case $N_1^* = N_2$, as shown in Fig. 3(e). The S^2 ICS circuit with the two-terminal ICS cell in Fig. 3(e) was first reported in [5] and called a magnetic switch (MS) power supply.

Generally, the S^2 ICS circuits with two-terminal and three-terminal ICS cells are functionally equivalent and, hence, they exhibit similar performance. Differences between them are mostly related to the transformer design. A S^2 ICS circuit with a two-terminal ICS cell requires at least one additional transformer winding (winding N_1^* in Fig. 3) and, consequently, it may require a larger transformer than the corresponding S^2 ICS circuit with a three-terminal ICS cell if winding N_1 is implemented by tapping the primary winding of the transformer. It should be noted that the S^2 ICS circuits with three-terminal ICS cells are limited to single-ended topologies such as the single-switch forward and flyback converters. On the other hand, the S^2 ICS circuits with two-terminal ICS cells can be implemented with any isolated dc/dc converter such as the two-switch and the full-bridge forward converters.

III. S^2 ICS CIRCUITS WITH VOLTAGE-DOUBLER RECTIFIER

Based on the classification of the S^2 ICS circuits with the wide-range FBR in Section II, two families of voltage-doubler S^2 ICS (VDS 2 ICS) converters are developed: a VDS 2 ICS family

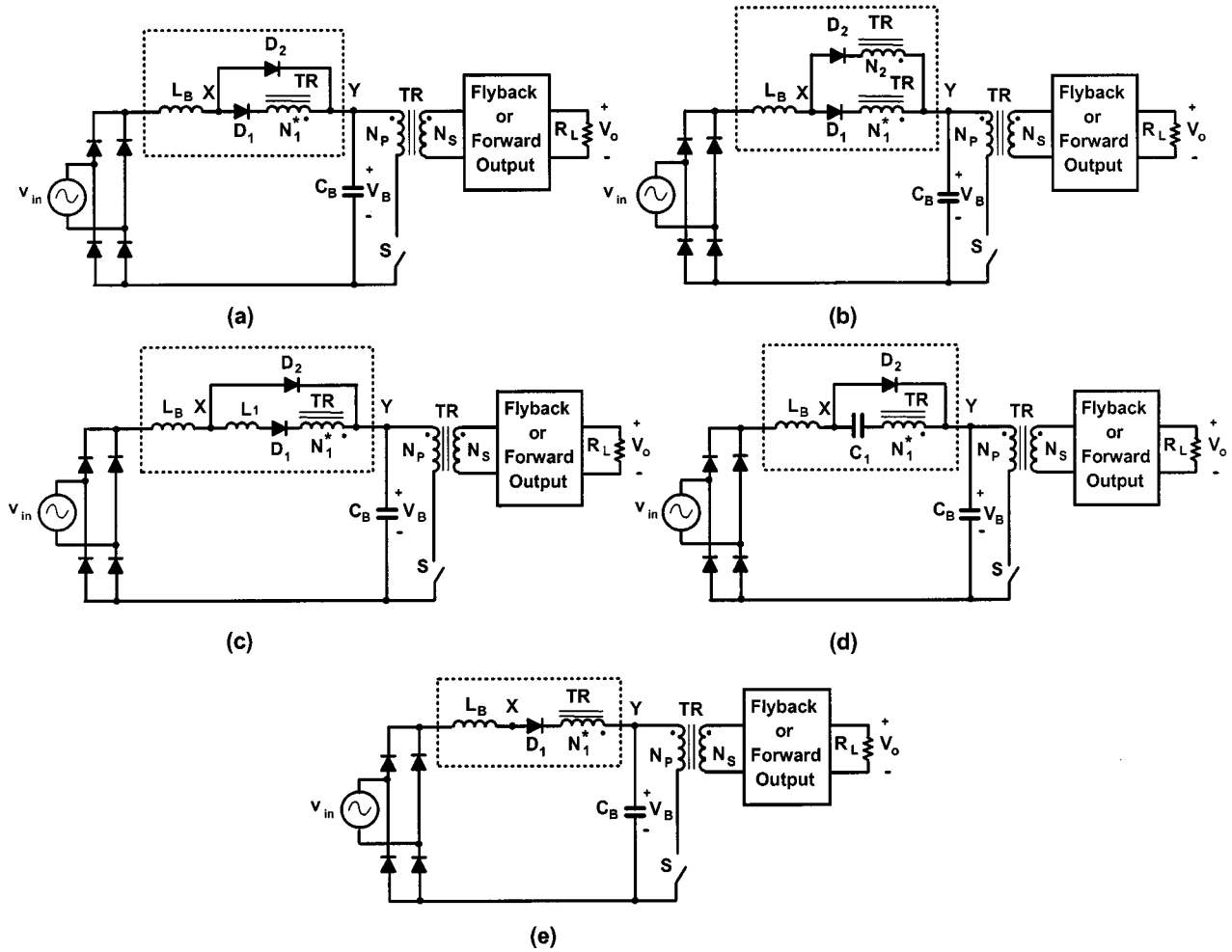


Fig. 3. S^2 ICS circuits with two-terminal ICS cells: (a) DCM ICS cell with winding N_1^* [6], (b) DCM ICS cell with windings N_1^* and N_2 , (c) inductive CCM ICS cell [10], (d) capacitive CCM ICS cell [5], and (e) simplified DCM ICS cell with windings N_1^* and N_2 for the case $N_1^* = N_2$ [5].

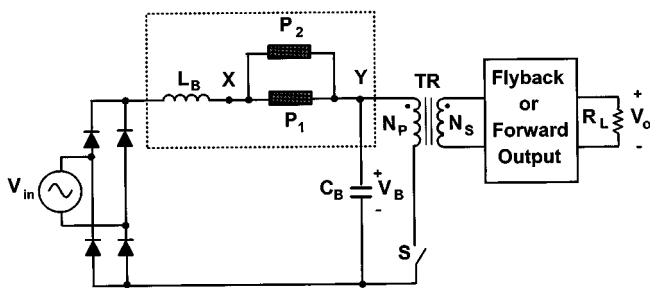


Fig. 4. S^2 ICS circuit with generalized two-terminal ICS cell.

with two-terminal ICS cells and a VDS^2 ICS family with three-terminal ICS cells.

A. VDS^2 ICS Family with Two-Terminal ICS Cells

Fig. 5 shows the generalized circuit diagram of the VDS^2 ICS family with two-terminal ICS cells. As shown in Fig. 5, a two-terminal ICS cell is inserted between the full-bridge rectifier and the energy-storage capacitors C_{B1} and C_{B2} in both the positive and negative rails. The two-terminal ICS cell in the negative rail is identical to the two-terminal ICS cell in the positive rail except

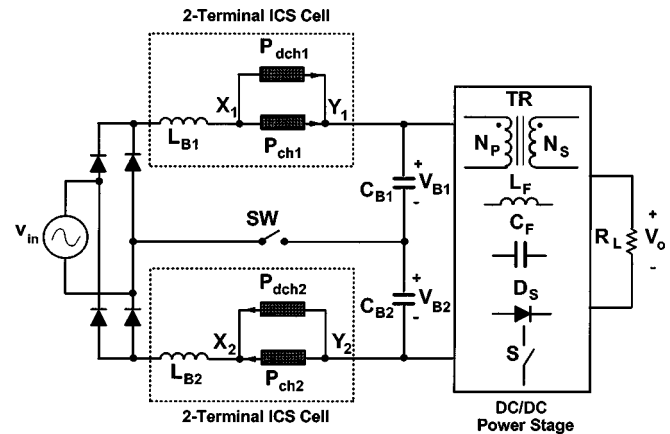
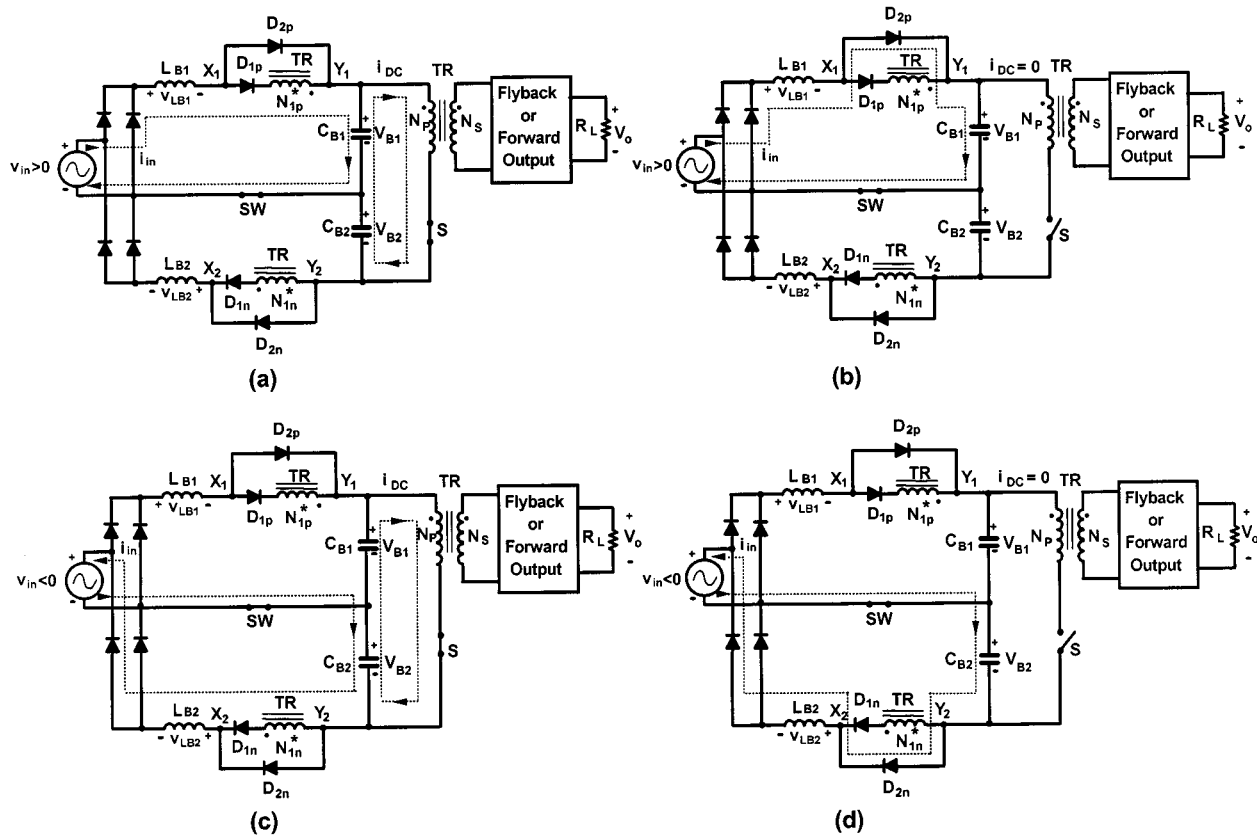


Fig. 5. Generalized circuit diagram of the VDS^2 ICS family with two-terminal ICS cells.

that the current direction of the boost inductor (L_{B2}) through its charging and discharging paths is referenced from node Y_2 to node X_2 . The two-terminal ICS cells in Fig. 5 can be any two-terminal ICS cell from Fig. 3. The dc/dc power stage in Fig. 5 can be any isolated power conversion topology such as the forward, flyback, half-bridge, and full-bridge topology. Switch


 Fig. 6. Operation modes of a VDS²ICS circuit with two-terminal ICS cells at low-line.

SW in Fig. 5 is the voltage-range-select switch. It can be implemented as a mechanical (manual) switch or as an electronic (autorange) switch.

To facilitate the understanding of operation of the VDS²ICS circuit with two-terminal ICS cells in Fig. 5, the operation modes of the circuit in Fig. 5 are illustrated on the example of a VDS²ICS circuit with the two-terminal ICS cells from Fig. 3(a) and with a single-ended dc/dc power stage. Figs. 6 and 7 show the operation modes of the proposed VDS²ICS circuit with two-terminal ICS cells in the low-line and high-line ranges, respectively. In the low-line range, range-select switch *SW* is closed and the front end operates in the voltage-doubler mode. As shown in Fig. 6(a) and (b), during a positive half cycle of the line voltage, the line current flows through the ICS cell in the positive rail. During the on-time of switch *S*, Fig. 6(a), the voltage across boost inductor L_{B1} is

$$v_{LB1} = v_{in} - \frac{V_B}{2} \cdot \left(1 - \frac{N_1^*}{N_P/2}\right) \quad (3)$$

where N_1^* is the number of turns of winding N_{1p}^* , $V_B = V_{B1} + V_{B2}$ and $V_{B1} \approx V_{B2} \approx V_B/2 > V_{in(pk)}$, where $V_{in(pk)}$ is the peak value of the line voltage. For proper operation, the number of turns of winding N_{1p}^* should be selected as

$$0 < N_1^* \leq N_P/2. \quad (4)$$

It should be noted that even when switch *S* is closed, the line current i_{in} cannot flow during the intervals when

$$v_{in} < \frac{V_B}{2} \cdot \left(1 - \frac{N_1^*}{N_P/2}\right). \quad (5)$$

As a result, the line current is distorted around the zero crossings of the line voltage, which produces harmonic distortions and reduces PF.

During the on-time of switch *S*, line current i_{in} flows through boost inductor L_{B1} , rectifier D_{1p} and winding N_{1p}^* , and the upper energy-storage capacitor C_{B1} . At the same time, the input current i_{DC} of the dc/dc power stage is supplied from energy-storage capacitors C_{B1} and C_{B2} , as indicated in Fig. 6(a).

When switch *S* turns off, Fig. 6(b), i_{DC} ceases to flow, whereas line current i_{in} commutates from the D_{1p} - N_{1p}^* path to rectifier D_{2p} . Because during the turn-off time of switch *S*

$$v_{LB1} = v_{in} - \frac{V_B}{2} < 0 \quad (6)$$

boost inductor L_{B1} discharges.

During a negative half cycle of the line voltage, the circuit in Fig. 5 operates in a similar manner as during a positive half cycle, except that the line current flows through the ICS cell in the negative rail as shown in Fig. 6(c) and (d).

When the circuit in Fig. 5 operates in the high-line range, range-select switch *SW* is open and the front end operates as a conventional full-bridge rectifier. As shown in Fig. 7, when operating as a conventional rectifier, the ICS cells in the positive and negative rails are connected in series as are the en-

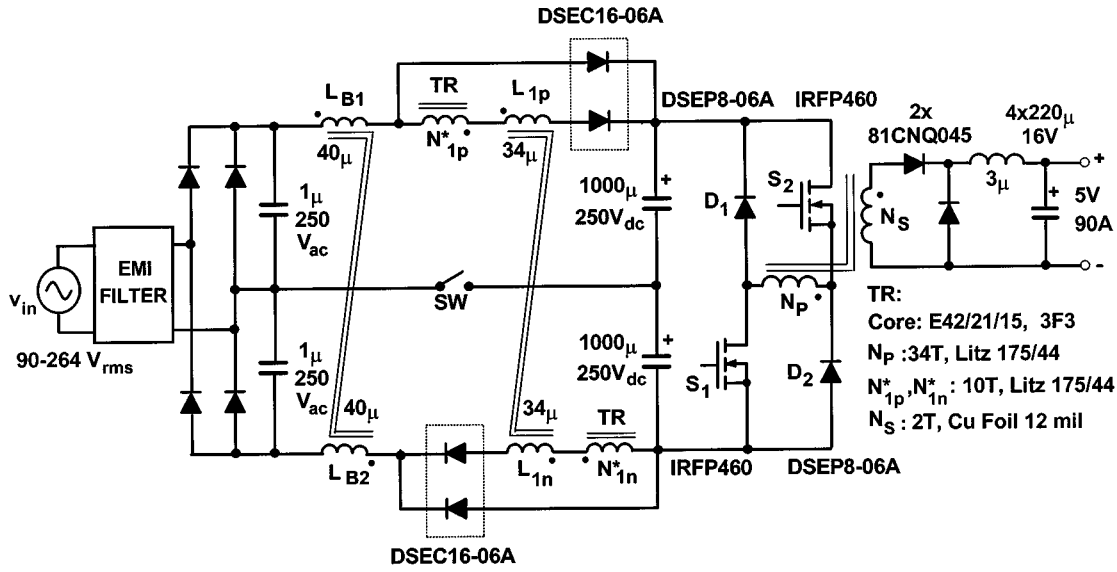


Fig. 9. Experimental circuit.

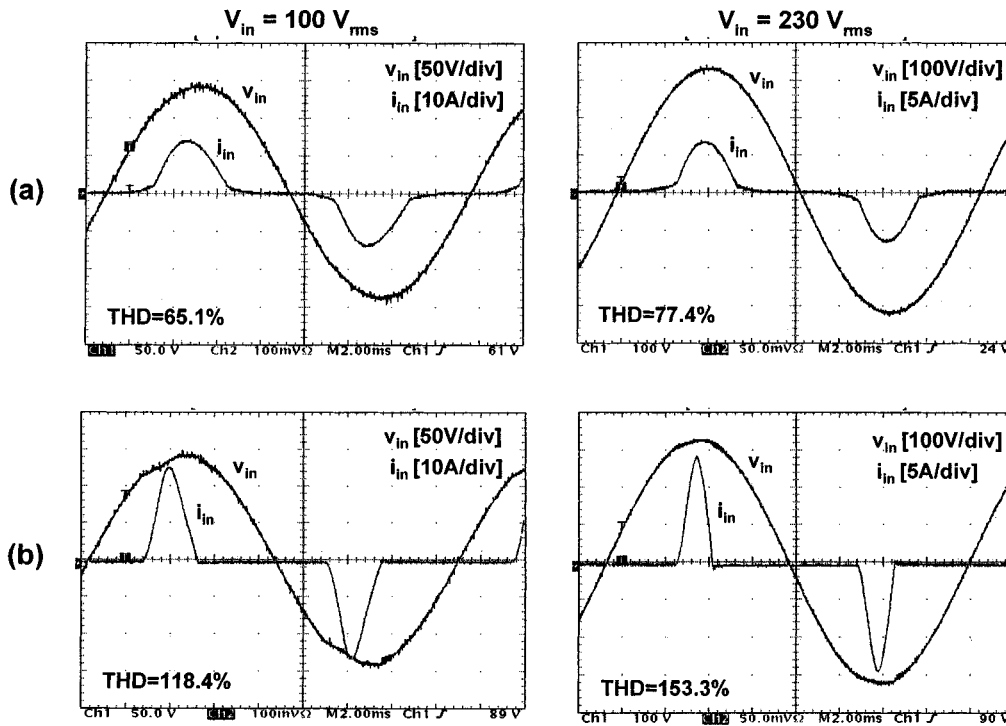


Fig. 10. Experimental line-voltage and line-current waveforms at full load ($V_o = 5\text{ V}$, $I_o = 90\text{ A}$): (a) with ICS front end and (b) without ICS front end.

in Fig. 8 do not have the same reference voltage, which may affect the design of the switch driver and the control feedback circuit requiring additional signal isolation.

Finally, it should be noted that in both VDS²ICS converters with two-terminal and three-terminal ICS cells, a single boost inductor can be placed on the ac-side of the rectifier bridge, or the two dc-side boost inductors can be coupled by winding them on the same magnetic core. In addition, in implementations of the ICS cells with inductor L_1 , Figs. 1(c) and 3(c), inductors L_1 in the positive and negative rails can be wound on a single core.

IV. EXPERIMENTAL RESULTS

The performance of the proposed VDS²ICS technique was verified experimentally on a 450-W (5-V/90-A) prototype circuit designed for the universal-line range (90–264 Vac). The circuit diagram of the power stage of the experimental circuit along with the values of the components is shown in Fig. 9. The experimental circuit is an implementation of the generalized circuit in Fig. 5 with the two-terminal ICS cells from Fig. 3(c). In addition, each pair of the two dc-side boost induc-

TABLE I
MEASURED PF, THD, V_B , AND EFFICIENCY AT FULL LOAD

V_{in} [V _{rms}]	PF	THD [%]	V_B [V]	η [%]
90	0.813	62.8	230	80.6
100	0.811	65.1	260	81.4
132	0.794	72.9	364	82.4
180	0.798	76.3	243	81.4
230	0.791	77.4	314	82.7
264	0.785	79.7	364	83.1

tors, L_{B1} and L_{B2} , and the two L_1 inductors, L_{1p} and L_{2p} , were wound on a single core. The dc/dc power stage was implemented as a two-switch forward converter. The control circuit was built around the low-cost integrated controller UC3842. The switching frequency was 70 kHz.

Measured line-voltage and line-current waveforms at nominal low line ($V_{in} = 100$ Vrms) and nominal high line ($V_{in} = 230$ Vrms), at full load ($I_o = 90$ A) are shown in Fig. 10(a). The measured individual line-current harmonics are well below the IEC 1000-3-2 Class-D limits and the corresponding Japanese standard limits, i.e., they have more than 15% margin for both the nominal high line and low line. To illustrate the improvement of the line current waveforms, measured line-voltage and line-current waveforms obtained on the same circuit without ICS (the two-terminal ICS cells removed from the circuit) are shown in Fig. 10(b). Table I summarizes the full-load PF, THD, total energy-storage-capacitor voltage V_B , and efficiency measurements that include the input-filter losses. The maximum total bulk-capacitor voltage was $V_{Bmax} = 435$ V, which was obtained at high line and 12-A load current.

Compared to the S^2 ICS circuit with the conventional wide-range full-bridge rectifier, the proposed VDS^2 ICS circuit has significantly lower total energy-storage-capacitor voltage and considerably higher efficiency, which is the result of the significantly narrower bulk-capacitor voltage range of the VDS^2 ICS circuit. Furthermore, compared to the conventional circuit with the voltage-doubler-rectifier front end without ICS, it can be seen that the proposed VDS^2 ICS circuit can be implemented by a simple modification of the VDR circuit without ICS. The overall efficiency of the VDS^2 ICS circuit is only slightly lower (around 1%) than the efficiency of the VDR counterpart without ICS, whereas, the VDS^2 ICS circuit meets the IEC 1000-3-2 Class D limits and the corresponding Japanese standard limits with enough margin.

V. CONCLUSION

A new single-stage input-current-shaping (S^2 ICS) technique for power supplies with a voltage-doubler-rectifier front end is proposed. The proposed technique significantly improves the performance of the S^2 ICS power supplies for universal-line (90–270-Vac) applications with a hold-up time requirement. Specifically, the variation range of the storage-capacitor voltage is reduced by approximately two times compared to the corresponding S^2 ICS circuits with the conventional wide-range

full-bridge rectifier. Consequently, energy-storage capacitors with the same total capacitance and with half of the voltage rating can be used as in the conventional S^2 ICS counterpart. In addition, the proposed technique improves the efficiency of the dc/dc output stage compared to the conventional S^2 ICS technique.

With the proposed ICS technique the existing power supplies with a voltage-doubler rectifier front end without input current shaping can be easily modified to meet the IEC 1000-3-2 and/or corresponding Japanese line-current-harmonic standards.

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