Performance Evaluation of Bridgeless PFC Boost Rectifiers

Laszlo Huber, Member, IEEE, Yungtaek Jang, Senior Member, IEEE, and Milan M. Jovanović, Fellow, IEEE

Abstract—In this paper, a systematic review of bridgeless power factor correction (PFC) boost rectifiers, also called dual boost PFC rectifiers, is presented. Performance comparison between the conventional PFC boost rectifier and a representative member of the bridgeless PFC boost rectifier family is performed. Loss analysis and experimental efficiency evaluation for both CCM and DCM/CCM boundary operations are provided.

Index Terms—Bridgeless power factor correction (PFC), common-mode noise, continuous-conduction mode (CCM), discontinuous-conduction mode (DCM)/CCM boundary, dual-boost PFC rectifier, single-phase rectifier.

I. INTRODUCTION

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AST-ESCALATING and extremely challenging high-efficiency requirements for ac/dc power supplies for notebooks, desktop computers, workstations, and servers, spelled out in the U.S. Environmental Protection Agency (EPA) Energy Star [1] and climate savers computing initiative [2] documents, are forcing designers to look for any possible opportunity to minimize power losses. Recently, in an effort to improve the efficiency of the front-end PFC rectifiers, many power supply manufacturers and some semiconductor companies have started looking into bridgeless PFC circuit topologies. Generally, the bridgeless PFC topologies, also referred to as dual-boost PFC rectifiers, may reduce the conduction loss by reducing the number of semiconductor components in the line-current path.

So far, a number of bridgeless PFC boost rectifier implementations and their variations have been proposed [3]–[23]. In this paper, a systematic review of the bridgeless PFC boost rectifier implementations that have received the most attention is presented. Performance comparison between the conventional PFC boost rectifier and a representative member of the bridgeless PFC boost rectifier family is performed. Loss analysis and experimental efficiency evaluation for both continuous-conduction mode (CCM) and discontinuous-conduction mode (DCM)/CCM boundary operations are provided.

II. REVIEW OF BRIDGELESS PFC BOOST RECTIFIERS

The basic topology of the bridgeless PFC boost rectifier [3]–[17] is shown in Fig. 1. Compared to the conventional PFC boost rectifier, shown in Fig. 2, one diode is eliminated from the line-current path, so that the line current simultaneously flows through only two semiconductors, as shown in Fig. 3, resulting in reduced conduction losses. However, the bridgeless PFC boost rectifier in Fig. 1 has significantly larger common-mode noise than the conventional PFC boost rectifier [21]–[23]. In fact, in the conventional PFC boost rectifier, the output ground is always connected to the ac source through the full-bridge rectifier (slow-recovery diodes and in Fig. 2), whereas, in the bridgeless PFC boost rectifier in Fig. 1, the output ground is connected to the ac source only during a positive half-line cycle, through the body diode of switch \( S_1 \), as shown in Fig. 3(a), while during a negative half-line cycle the output ground is pulsating relative to the ac source with a high frequency (HF) and with an amplitude equal to the output voltage, as follows from Fig. 3(b). This HF pulsating voltage source charges and discharges the equivalent parasitic capacitance between the output ground and the ac line ground, resulting in a significantly increased common-mode noise.

To reduce the common-mode noise of the bridgeless PFC boost rectifier in Fig. 1, i.e., to make it similar to that of the
conventional PFC boost rectifier, the topology of the bridgeless PFC boost rectifier in Fig. 1 needs to be modified to always provide a low-frequency (LF) path between the ac source and the positive or negative terminal of the output.

In Figs. 4 and 6, the modification of the basic bridgeless PFC boost rectifier is implemented by adding two diodes, $D_2$ and $D_4$. In addition, in Fig. 4, the common-source node of switches $S_1$ and $S_2$ is disconnected from the output ground. The circuit in Fig. 4 can be redrawn as shown in Fig. 5, which is the bridgeless PFC boost rectifier with a bidirectional switch [5], [17]. It should be noted that in Fig. 5, diodes $D_1$ and $D_3$ are fast-recovery diodes, whereas diodes $D_2$ and $D_4$ are slow-recovery diodes. During a positive half-line cycle, the ac source is connected to the output ground through slow-recovery diode $D_2$, and during a negative half-line cycle, the ac source is connected to the positive terminal of the output through slow-recovery diode $D_4$.

In Fig. 6, in addition to diodes $D_2$ and $D_4$, which are slow-recovery diodes, a second inductor is also added, resulting in two dc/dc boost circuits, one for each half-line cycle [18], [19]. A positive half-line cycle, the first dc/dc boost circuit, $L_{B1} - S_1 - D_1$, is active through diode $D_1$, which connects the ac source to the output ground. During a negative half-line cycle, the second dc/dc boost circuit, $L_{B2} - S_2 - D_2$, is active through diode $D_3$, which connects the ac source to the output ground.

It should be noted that switches $S_1$ and $S_2$, in both bridgeless PFC boost rectifiers in Figs. 5 and 6, can be driven with the same PWM signal, which significantly simplifies the implementation of the control circuit. The drawback of the bridgeless PFC boost rectifier in Fig. 5 is that it requires an additional gate-drive transformer. The drawback of the bridgeless PFC boost rectifier in Fig. 6 is that it requires two inductors. However, it should also be noted that two inductors compared to a single inductor have better thermal performance.

Fig. 7 shows a variation of the bridgeless PFC boost rectifier with two dc/dc boost circuits in Fig. 6 [20]. Because of the position of switches $S_1$ and $S_2$, this topology is called pseudo totem-pole bridgeless PFC boost rectifier [20]. During a positive half-line cycle, dc/dc boost circuit $L_{B1} - S_1 - D_1$ is active through diode $D_1$, which connects the ac source to the output ground. During a negative half-line cycle, dc/dc boost circuit $L_{B2} - S_2 - D_2$ is active through diode $D_3$, which connects the ac source to the positive terminal of the output. It should be noted that switches $S_1$ and $S_2$ in Fig. 7 cannot be driven with
requires an iso-
(Fig. 2), only one
are implemented with the
and
. Because of the totem-pole arrangement of
and
and switch
and
in Figs. 9 and 10 is employed. The
is the line frequency.
[17]. Because of the po-
in Fig. 2, also consists
in Fig. 6,
line voltage and a 300-W DCM/CCM boundary imple-
is the rms value of
and
, where
the position of diode
the same PWM signal. Furthermore, switch
requires an iso-
lated gate drive. Therefore, the bridgeless PFC boost rectifier in
Fig. 7 requires a more complex control and drive circuit and,
consequently, it is less attractive for practical implementation
than its counterpart in Fig. 6.

Finally, Fig. 8 shows a modification of the basic bridgeless
PFC boost rectifier from Fig. 1 which is obtained by exchanging
the position of diode
and switch
[17]. Because of the position
of the two switches, the topology in Fig. 8 is called the
totem-pole bridgeless PFC boost rectifier. It should be noted
that diodes
and
are slow-recovery diodes. During a posi-
tive half-line cycle, the ac source is connected to the output
ground through diode
, and during a negative half-line cycle,
the ac source is connected to the positive terminal of the output
through diode
. Because of the totem-pole arrangement
of the switches, the bridgeless PFC boost rectifier in Fig. 8 can
only work in DCM and at DCM/CCM boundary. In fact, the re-
verse-recovery performance of the body diodes of the switches
makes CCM operation of the bridgeless PFC boost rectifier in
Fig. 8 impractical. Even the DCM/CCM boundary operation is
not practical because during start-up and load transients, the rec-
tifier may operate in CCM. In addition, the totem-pole bridge-
less PFC boost rectifier in Fig. 8 requires a complex control and
drive circuit. With the exception of the totem-pole bridgeless
PFC boost rectifier in Fig. 8, the other bridgeless PFC boost rec-
tifiers in Figs. 5–7 can operate in both CCM and DCM.

It can be concluded that only two bridgeless PFC boost recti-
tifier topologies are suitable for practical implementation: the
bridgeless PFC boost rectifier with the bidirectional switch in
Fig. 5 and the bridgeless PFC boost rectifier with two dc/dc
boost circuits in Fig. 6. In Sections III and IV, the bridgeless
PFC boost rectifier in Fig. 6 is selected for performance com-
parison with the conventional PFC boost rectifier because its
gate drive circuits are referenced to ground, and, therefore, it is
less noise sensitive.

III. POWER LOSS CALCULATIONS

The power loss calculations were performed using Mathcad
with the following assumptions.
1) The input voltage is sinusoidal, i.e.,

\[ v_{\text{in}} = \sqrt{2}V_{\text{in}} \sin(2\pi f_L t) \]

where

\( V_{\text{in}} \)

is the rms value of

\( f_L \)

is the line frequency.

2) The input current waveform follows the input voltage

\[ i_{\text{in}} = \sqrt{2}I_{\text{in}} \sin(2\pi f_L t) \]

where

\( I_{\text{in}} \)

is the rms value of the line current is determined as

\[ I_{\text{in}} = P_o/\left(\eta \cdot V_{\text{in}}\right), P_o \text{ being the output power and } \eta \text{ is the assumed efficiency.} \]

3) The input voltage and input current are considered as con-

\( f_{\text{sw}} \approx f_L. \)

stant during a switching cycle (quasi-static approach) be-

\( f_{\text{sw}} \)

cause the switching frequency is much larger than the line

\( f_L \)

frequency, i.e.,

4) For a fair comparison, it is assumed that the boost switch

\( S_B \)

in Fig. 2, consists of two MOSFETs connected in parallel, while each switch

\( S_1 \) and \( S_2 \) in Fig. 6,

comprises only one MOSFET. Similarly, the boost diode of

\( D_B \)

the conventional PFC rectifier, \( D_{B1} \) in Fig. 2, also consists

\( D_{B2} \)

of two diodes connected in parallel, while each diode of

\( D_1 \) and \( D_2 \) in Fig. 6,

comprises a single diode.

The power loss calculation procedure is described in details
in the Appendix.

Key components of the CCM and DCM/CCM boundary
bridgeless PFC boost rectifiers used in the loss calculations are
shown in Figs. 9 and 10, respectively. As can be seen in
Figs. 9 and 10, diodes \( D_3 \) and \( D_4 \) are implemented with the
two bottom diodes of the full-bridge rectifier D15XB60. In the
corresponding conventional PFC boost rectifiers, the whole
full-bridge rectifier D15XB60 is used for diodes \( D_1 - D_4 \)
(Fig. 2), whereas, for boost inductor \( L_B \) (Fig. 2), only one
boost inductor \( L_{B1}/L_{B2} \) in Figs. 9 and 10 is employed. The
input filter and the bulk capacitor in the conventional PFC boost
rectifiers are identical to those in the bridgeless PFC boost recti-

Breakdown of losses of a 750-W CCM implementation at
85-V_{\text{rms}} line voltage and a 300-W DCM/CCM boundary imple-
mentation at 90-V_{\text{rms}} line voltage, with a 400-V output voltage,
are presented in Tables I and II, respectively. These power levels
are power levels of the experimental circuits. For the boost switches, the IPP60R099CS MOSFETs were used,
similarly as in the experimental circuits. It follows from
Tables I and II that the major loss components in both CCM and
DCM/CCM boundary implementations are the input diodes and
the boost switches. In CCM implementation, the loss of the EMI
filter is also significant. The efficiency improvement is 0.46%
in CCM implementation and 0.69% in DCM/CCM boundary
implementation. Geneerally, the efficiency could be further im-
proved by using MOSFETs with lower on-resistance.
IV. EXPERIMENTAL RESULTS

As the efficiency improvement of the bridgeless PFC boost rectifier over the conventional PFC boost rectifier is predominantly limited by the on-resistance of the boost switches, in the efficiency calculations different MOSFETs with different on-resistances were used. The calculated efficiencies for the CCM and DCM/CCM boundary PFC boost rectifiers are presented in Figs. 11 and 12, respectively.

In the efficiency calculations for the CCM PFC boost rectifiers, four MOSFETs with different on-resistances shown in Fig. 10 are used. As shown in Fig. 12, for all MOSFETs except for the SPP07N65C3, which has the highest $R_{DSon}$, the efficiency of the bridgeless PFC boost rectifier is higher than that of the conventional PFC boost rectifier over the entire calculated output power range. The SPP11N65C3 MOSFET, which has an $R_{DSon} = 380 \, \text{m} \Omega$, can be considered as the borderline to achieve an efficiency improvement by using the bridgeless PFC boost rectifier compared to the conventional boost PFC rectifier in the whole calculated output power range. It is also shown in Fig. 12 that at output power levels above approximately 200 W, the employment of the larger MOSFET IPW60R044CS in TO-247 package results in the highest efficiency. However, the employment of the IPP60R099CS MOSFET yields the most uniform high efficiency in the whole calculated output power range. It can be concluded from Fig. 12 that the IPP60R099CS MOSFET used in the bridgeless PFC boost rectifier operating at the DCM/CCM boundary, exhibits an optimal balance between the conduction losses and the switching losses in the calculated output power range.

Fig. 9. Circuit diagram of the experimental CCM bridgeless PFC boost rectifier.

Fig. 10. Circuit diagram of the experimental DCM/CCM boundary bridgeless PFC boost rectifier.

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IV. EXPERIMENTAL RESULTS

A 750-W, constant switching frequency (110 kHz) CCM experimental circuit and a 300-W, variable switching frequency (85–400 kHz) DCM/CCM boundary experimental circuit were built for the universal ac-line input (90–264 Vrms) with a 400-V output. The circuit diagram of the CCM and DCM/CCM boundary bridgeless PFC experimental circuit is shown in Figs. 9 and 10, respectively. Because of cost concerns and high light-load efficiency requirements, in both experimental circuits, the IPP60R099CS MOSFET was used as the boost switch. The control circuit of the CCM implementation is based on the ICE1PCS01 controller IC from Infineon, whereas the control circuit of the DCM/CCM boundary implementation is based on a controller ASIC similar to the NCP1601 controller IC from ON Semiconductor. Both control circuits are very output power, unlike the bridgeless PFC boost rectifier, which shows an efficiency improvement above 550-W output power when using a larger MOSFET. This is due to the increased switching losses. In fact, at low power levels, the efficiency of both the conventional and bridgeless PFC boost rectifiers is dominated by switching losses, whereas, at high power levels, the efficiency of both rectifiers is dominated by conduction losses. Since the conventional PFC boost rectifier employs both switches throughout the whole line cycle, the effective switch capacitance is twice as high as that of the bridgeless PFC boost rectifier, where each switch is employed only during one half of the line cycle, resulting in less overall switching losses. It can be concluded from Fig. 11 that for high efficiency of the PFC boost rectifier operating in CCM, at output power levels above 600 W, the bridgeless PFC boost rectifier using the IPW60R044CS MOSFETs is the preferred solution, whereas, at output power levels below 400 W, the bridgeless PFC boost rectifier using the IPP60R099CS MOSFETs is recommended. If switches with equal or higher $R_{DSon}$ than that of the SPP20N65C3 MOSFET are employed, the conventional boost PFC circuit is the better choice.

In the efficiency calculations for the DCM/CCM boundary PFC boost rectifiers, four MOSFETs with different on-resistances shown in Fig. 10 are used. As shown in Fig. 12, for all MOSFETs except for the SPP07N65C3, which has the highest $R_{DSon}$, the efficiency of the bridgeless PFC boost rectifier is higher than that of the conventional PFC boost rectifier over the entire calculated output power range. The SPP11N65C3 MOSFET, which has an $R_{DSon} = 380 \, \text{m} \Omega$, can be considered as the borderline to achieve an efficiency improvement by using the bridgeless PFC boost rectifier compared to the conventional boost PFC rectifier in the whole calculated output power range. It is also shown in Fig. 12 that at output power levels above approximately 200 W, the employment of the larger MOSFET IPW60R044CS in TO-247 package results in the highest efficiency. However, the employment of the IPP60R099CS MOSFET yields the most uniform high efficiency in the whole calculated output power range. It can be concluded from Fig. 12 that the IPP60R099CS MOSFET used in the bridgeless PFC boost rectifier operating at the DCM/CCM boundary, exhibits an optimal balance between the conduction losses and the switching losses in the calculated output power range.

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In the efficiency calculations for the DCM/CCM boundary PFC boost rectifiers, four MOSFETs with different on-resistances shown in Fig. 10 are used. As shown in Fig. 12, for all MOSFETs except for the SPP07N65C3, which has the highest $R_{DSon}$, the efficiency of the bridgeless PFC boost rectifier is higher than that of the conventional PFC boost rectifier over the entire calculated output power range. The SPP11N65C3 MOSFET, which has an $R_{DSon} = 380 \, \text{m} \Omega$, can be considered as the borderline to achieve an efficiency improvement by using the bridgeless PFC boost rectifier compared to the conventional boost PFC rectifier in the whole calculated output power range. It is also shown in Fig. 12 that at output power levels above approximately 200 W, the employment of the larger MOSFET IPW60R044CS in TO-247 package results in the highest efficiency. However, the employment of the IPP60R099CS MOSFET yields the most uniform high efficiency in the whole calculated output power range. It can be concluded from Fig. 12 that the IPP60R099CS MOSFET used in the bridgeless PFC boost rectifier operating at the DCM/CCM boundary, exhibits an optimal balance between the conduction losses and the switching losses in the calculated output power range.
simple because the controller ICs do not require the detection of the positive and negative half cycles of the line voltage. The two boost switches are simultaneously driven with the same gate drive signal from the corresponding controller IC. For current sensing, current transformers were used.

To compare the performance of the bridgeless and conventional PFC boost rectifiers, the same prototype hardware was used. In the conventional PFC rectifier, boost switch $S_B$ in Fig. 2 was implemented with the two boost switches $S_1$ and $S_2$ in Figs. 9 and 10 connected in parallel, and boost diode $D_B$ in Fig. 2 was implemented with the two boost diodes $D_1$ and $D_2$ in Figs. 9 and 10 connected in parallel. For boost inductor $L_B$ in Fig. 2, only one boost inductor $L_{B1}$ in Figs. 9 and 10 was employed.

Efficiency measurements are presented in Figs. 13 and 14. It can be seen in Fig. 13 that the CCM bridgeless PFC boost rectifier exhibits an improved efficiency of 1%–2% at output power levels 350–750 W, around 3.5% at 150-W (20% load),

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### TABLE I
BREAKDOWN OF LOSSES OF 750-W CCM PFC BOOST RECTIFIER

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<tbody>
<tr>
<td>Conventional PFC</td>
<td>4.46</td>
<td>1.43</td>
<td>4.45</td>
<td>2.30</td>
<td>0.2</td>
<td>1.15</td>
<td>2.48</td>
<td>15.8</td>
<td>12.58</td>
<td>44.85</td>
</tr>
<tr>
<td>Bridgeless PFC</td>
<td>4.46</td>
<td>1.43</td>
<td>8.90</td>
<td>1.15</td>
<td>0.1</td>
<td>1.15</td>
<td>3.32</td>
<td>7.9</td>
<td>12.58</td>
<td>41.0</td>
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### TABLE II
BREAKDOWN OF LOSSES OF 300-W DCM/CCM BOUNDARY PFC BOOST RECTIFIER

<table>
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</thead>
<tbody>
<tr>
<td>Conventional PFC</td>
<td>0.63</td>
<td>0.64</td>
<td>0.85</td>
<td>0.22</td>
<td>0.94</td>
<td>1.19</td>
<td>5.88</td>
<td>0.75</td>
<td>11.1</td>
<td>96.43</td>
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<tr>
<td>Bridgeless PFC</td>
<td>0.63</td>
<td>0.64</td>
<td>1.7</td>
<td>0.11</td>
<td>0.94</td>
<td>1.19</td>
<td>2.94</td>
<td>0.75</td>
<td>8.9</td>
<td>97.12</td>
</tr>
</tbody>
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Fig. 11. (Dashed lines) Calculated efficiency of conventional PFC boost rectifier in Fig. 2 and (solid lines) bridgeless PFC boost rectifier in Fig. 6 operating in CCM.

Fig. 12. (Dashed lines) Calculated efficiency of conventional PFC boost rectifier in Fig. 2 and (solid lines) bridgeless PFC boost rectifier in Fig. 6 operating at DCM/CCM boundary.
and over 7% at 50-W output power at worst case (low line) compared to its conventional CCM counterpart. It follows from Fig. 14 that the DCM/CCM boundary bridgeless PFC boost rectifier improves the worst-case efficiency (low line) by 0.8% at full load and by almost 5% at 60-W (20% load) compared to its conventional DCM/CCM counterpart. It can be concluded from Figs. 13 and 14 that the DCM/CCM boundary implementation of the bridgeless PFC boost rectifier has a slightly better efficiency than the CCM implementation.

It should be noted that the measured efficiencies in Fig. 13 are in good agreement with the calculated efficiencies in Fig. 11 at output power levels above 350 W, whereas the measured efficiencies in Fig. 14 are in good agreement with the calculated efficiencies in Fig. 12 at output power levels above 100 W. At lower output power levels, the measured efficiencies are lower than the calculated efficiencies. This can be explained by the fact that at lower power levels, the turn-off switching losses, which were not taken into account in the efficiency calculations, cannot be neglected. It should be also noted that the mismatch between the measured and calculated efficiencies at lower power levels is more pronounced for the conventional PFC boost rectifier, which is the result of the elevated switching losses as two MOSFETs operate in parallel. Nevertheless, the general conclusions and the efficiency trends obtained by the analysis of the calculated efficiencies are still valid.

Measured line voltage and line current waveforms of the bridgeless PFC boost rectifier in Fig. 6 at full load, at low line, and high line are, respectively, shown in Figs. 15 and 16 for the CCM implementation and in Figs. 17 and 18 for the DCM/CCM boundary implementation. It follows from Figs. 15–18 that the quality of the line current in CCM implementation is slightly
better than that in the DCM/CCM boundary implementation, especially at high line. The distortion in the line current waveform in the DCM/CCM boundary implementation is caused by the nonuniform valley switching of the MOSFETs. Nevertheless, the line current in the DCM/CCM boundary implementation still meets the standards for the line current harmonics such as EN 61000-3-2. The measured PF and THD at full load and low line are 99.9% and 3.5% for the CCM implementation and 99.5% and 7.4% for the DCM/CCM boundary implementation. The measured PF and THD at full load and high line are 99.1% and 7.9% for the CCM implementation and 90.9% and 25.1% for the DCM/CCM boundary implementation.

Figs. 17 and 18 include also the measured boost-inductor current waveform. The switching frequency variation at full load, low line and high line is 85–130 kHz and 60–400 kHz, respectively. As shown in Fig. 18, at full load and high line, around the peak value of the line voltage, the boost inductor slightly enters the CCM operation, which is the result of the limitation of the controller IC. It should be noted in Figs. 17 and 18 that the controller IC. It should be noted in Figs. 17 and 18 that the

Fig. 17. Measured line voltage, line current, and boost-inductor current waveforms of bridgeless PFC boost rectifier in Fig. 6 operating at DCM/CCM boundary at full load (300 W) at 90-Vrms line voltage (PF = 99.5%, THD = 7.4%).

Fig. 18. Measured line voltage, line current, and boost-inductor current waveforms of bridgeless PFC boost rectifier in Fig. 6 operating at DCM/CCM boundary at full load (300 W) at 264-Vrms line voltage (PF = 90.9%, THD = 25.1%).

V. SUMMARY

The bridgeless PFC boost rectifiers, also called the dual-boost PFC rectifiers, compared to the conventional PFC boost rectifier, generally, improve the efficiency of the front-end PFC stage by eliminating one diode forward-voltage drop in the line-current path. The basic bridgeless PFC boost rectifier [3] is not a practical solution because it has significantly larger common mode noise than the conventional PFC boost rectifier. Today, two topologies can be considered as attractive for practical implementation: the bridgeless PFC boost rectifier with the bidirectional switch [5] and the bridgeless PFC boost rectifier with two dc/dc boost circuits [18]. In this paper, the bridgeless PFC boost rectifier with two dc/dc boost circuits is selected as a representative member of the bridgeless PFC boost rectifier family for performance comparison with the conventional PFC boost rectifier.

A 750-W, constant switching frequency (110 kHz) CCM experimental circuit and a 300-W, variable switching frequency (85–400 kHz) DCM/CCM boundary experimental circuit were built for the universal ac-line input (90–264 V) with a 400-V output. The CCM bridgeless PFC boost rectifier had an improved efficiency of 1%–2% at output power levels 350–750 W and around 3.5% at 20% load, whereas the DCM/CCM boundary bridgeless PFC boost rectifier improved the efficiency by 0.8% at full load and by almost 5% at 20% load at worst case (low line) compared to their respective conventional CCM and DCM/CCM boundary counterparts. It was found that the DCM/CCM boundary implementation had a slightly better efficiency than the CCM implementation. However, the quality of the line current in the CCM implementation was slightly better than that in the DCM/CCM boundary implementation, especially at high line.

APPENDIX

In calculation of power losses, the first step is to obtain the waveform of the boost inductor current. In CCM operation, the waveform of the boost inductor current during a switching cycle can be approximated as shown in Fig. 19. The average boost inductor current in the kth switching cycle during a half line cycle is equal to the input current in the kth switching cycle, i.e.,

$$i_{LB,ave}[k] = |i_{in}[k]| = I_{in,1k} \sin(2\pi f_L \cdot k T_{sw})$$

$$k = 1, \ldots, k_{MAX}$$ (1)
The relevant currents for calculation of conduction losses are the rms current of the boost inductor, boost switch, and output capacitor; and the average current of the boost diode and input diode, which are determined in the $k$th switching cycle as [25]

$$i_{LB,rms}[k] = |i_{in}[k]| \cdot \sqrt{1 + \frac{1}{3} \left(\frac{\Delta L_B[k]}{2i_{in}[k]}\right)^2} \quad (5)$$

$$i_{SB,rms}[k] = \sqrt{D[k] \cdot i_{LB,rms}[k]} \quad (6)$$

$$i_{CB,rms}[k] = \sqrt{i_{LB,rms}[k]^2 - i_{SB,rms}[k]^2 - T_o^2} \quad (7)$$

$$i_{DB,ave}[k] = (1 - D[k]) \cdot |i_{in}[k]| \quad (8)$$

$$i_{Din,ave}[k] = |i_{in}[k]| \quad (9)$$

respectively. The corresponding rms and average currents during a half line cycle are as follows:

$$I_{XB,rms} = \sqrt{2f_L \cdot \sum_{k=1}^{k_{max}} i_{XB,ave}[k] \cdot T_{sw}, X \in \{L, S, D, C\}} \quad (10)$$

$$I_{DY,ave} = 2f_L \cdot \sum_{k=1}^{k_{max}} i_{DY,ave}[k] \cdot T_{sw}, Y \in \{B, i_{in}\} \quad (11)$$

In DCM/CCM boundary operation, the boost inductor current waveform during a switching cycle is shown in Fig. 20. At DCM/CCM boundary, the PFC boost rectifier operates with variable switching frequency and constant on-time. It should be noted that valley switching of the boost switch, i.e., turn-on with zero-voltage switching (ZVS) can be easily achieved. However, it can be assumed that the resonant interval, i.e., the time it takes the voltage of the boost switch output capacitance to resonate down to its valley is negligible with respect to the switching period. The constant on-time is determined as

$$T_{on} = \frac{D_{min}}{f_{sw,min}} \quad (12)$$

where

$$D_{min} = 1 - \sqrt{2} \frac{V_{in}}{V_o} \quad (13)$$

is the minimum duty cycle obtained at the peak of the input voltage, and

$$f_{sw,min} = \frac{V_{in}D_{min}}{2L_B I_{in}} \quad (14)$$

is the corresponding minimum switching frequency. The off-time in the $k$th switching cycle during a half line cycle is determined as

$$T_{off}[k] = \frac{|i_{in}[k]| \cdot T_{on}}{V_o - |i_{in}[k]|} \quad (15)$$

where

$$|i_{in}[k]| = \sqrt{2} V_{in} \sin(2\pi f_L t_k) \quad (16)$$

where $T_{sw} = 1/f_{sw}$ is the switching period, and $k_{max}$ is the number of switching cycles in a half line cycle ($k_{max}$ is the greatest integer of $f_{sw}/2f_L$). The change of the boost inductor current in the $k$th switching cycle is determined as

$$\Delta i_{LB}[k] = \frac{V_{in}[k]}{L_{B}[k]} \cdot D[k] \cdot T_{sw} \quad (2)$$

where

$$D[k] = 1 - \frac{|i_{in}[k]|}{V_o} \quad (3)$$

is the duty cycle, and

$$L_{B}[k] = L_{B0} \cdot \mu_{eff}[k] / \mu_0, \mu_{eff}[k] = f(i_{in}[k]) \quad (4)$$

is the boost inductance in the $k$th switching cycle. It should be noted that the boost inductance varies with the input current because the CCM boost inductor is implemented with high-flux powder cores [24].
being the instant when the inductor current has its peak value during the $k$th switching cycle, i.e.,

$$t_k = \frac{T_{on}}{k} \left( k = 1, \ldots, k_{\text{max}} \right).$$

(17)

In (17), the switching period in the $k$th switching cycle is determined as

$$T_{\text{sw}}[k] = T_{\text{on}} + T_{\text{off}}[k].$$

(18)

The rms current of the boost inductor in the $k$th switching cycle during a half line cycle is obtained as [25]

$$i_{L_{\text{B, rms}}}[k] = \frac{i_{L_{\text{B, pk}}}[k]}{\sqrt{3}} = \frac{2\sqrt{2}i_{L_{\text{in}}}[k]}{\sqrt{3}} (2\pi f_{L} t_k),$$

(19)

whereas the corresponding rms current during a half-line cycle is obtained as

$$I_{L_{\text{B, rms}}} = \sqrt{2 f_{L} \sum_{k=1}^{k_{\text{max}}} i_{L_{\text{B, rms}}}[k] \cdot T_{\text{sw}}[k]}.$$  

(20)

It can be easily shown that

$$I_{L_{\text{B, rms}}} = \frac{2}{\sqrt{3}} \cdot I_{L_{\text{in}}}.$$  

(21)

The rms and average currents of other components relevant for the calculation of the conduction losses during a half line cycle are obtained as

$$I_{S_{\text{B, rms}}} = \sqrt{2 f_{L} \sum_{k=1}^{k_{\text{max}}} i_{S_{\text{B, rms}}}[k] \cdot T_{\text{on}}}$$

(22)

$$I_{C_{\text{B, rms}}} = \sqrt{2 f_{L} \sum_{k=1}^{k_{\text{max}}} i_{C_{\text{B, rms}}}[k] \cdot T_{\text{on}}} - I_{O}^2.$$  

(23)

$$I_{D_{\text{B, ave}}} = 2 f_{L} \sum_{k=1}^{k_{\text{max}}} i_{L_{\text{B, pk}}}[k] \cdot (T_{\text{sw}}[k] - T_{\text{on}})$$

(24)

$$I_{I_{\text{in, ave}}} = \frac{2\sqrt{2}}{\pi} \cdot I_{L_{\text{in}}}.$$  

(25)

It should be noted that, around the zero crossings of the line voltage, during a few switching cycles, the PFC boost rectifier operates in DCM, which was not taken into consideration above, when the boost-inductor current waveform was obtained. However, the operation in DCM around the zero crossings of the line voltage has negligible effect on the total waveform of the boost inductor current during a half-line cycle, and, therefore, its effect in the loss calculations can be neglected.

The rms-current-based conduction losses are calculated as $R_{\text{s}} \cdot I_{L_{\text{B, rms}}}^2$. In the calculation of the winding loss of the boost inductor, the skin and proximity effects were also taken into account by using Dowell’s approach [25], [26]. The average-current-based conduction losses, i.e., diode conduction losses are calculated by multiplying the average diode current during a half-line cycle with an average forward voltage drop of the diode, or, for a better accuracy, by multiplying the average diode current during each switching cycle with the corresponding forward voltage drop and then averaging during the half line cycle.

The calculation of switching losses includes the switching loss of the boost switches, the gate-drive losses, and the core loss of the boost inductor. The switching loss of the boost switches in CCM operation is based on the turn-on loss due to the effective capacitance of the MOSFET ($C_{\text{oss}} f_{\text{sw}} V_{DS, \text{avg}}/2$). The switching loss of the boost switches in DCM/CCM boundary operation is negligible due to the turn-on of the switches with valley switching. It should be noted that an accurate calculation of the turn-off losses of the boost switches can be performed only by using simulations, e.g., PSPICE or SIMPLIS, provided that reliable MOSFET models are available. However, generally, the turn-off losses of the boost switches can be neglected, especially in the DCM/CCM boundary operation with a capacitive turn-off snubber across the switch, which results in a significantly slower increase of the drain-source voltage. Finally, the core loss of the boost inductor is calculated by using the Steinmetz approach [25].

REFERENCES


Laszlo Huber (M’86) was born in Novi Sad, Yugoslavia, in 1953. He received the Dipl. Eng. degree from the University of Novi Sad, the M.S. degree from the University of Niš, Niš, Yugoslavia, and the Ph.D. degree from the University of Novi Sad in 1977, 1983, and 1992, respectively, all in electrical engineering.

From 1977 to 1992, he was an Instructor at the Institute for Power and Electronics, University of Novi Sad. In 1992, he joined the Virginia Power Electronics Center at Virginia Tech, Blacksburg, as a Visiting Professor. From 1993 to 1994, he was a Research Scientist at the Virginia Power Electronics Center. Since 1994, he has been a Senior Member of the R&D Staff at the Power Electronics Laboratory, Delta Products Corporation, Research Triangle Park, NC, the Advanced R&D unit of Delta Electronics, Inc., Taiwan, R.O.C., one of the world’s largest manufacturers of power supplies. His 30-year experience includes the analysis, simulation, and design of high-frequency, high-power-density, single-phase, and three-phase power processors; modeling, simulation, evaluation, and application of high-power semiconductor devices; and modeling, simulation, analysis, and design of analog and digital electronics circuits. He has published over 80 technical papers and holds four U.S. patents.

Yungtaek Jang (S’92–M’95–SM’01) was born in Seoul, Korea. He received the B.S. degree from Yonsei University, Seoul, Korea, in 1982, and the M.S. and Ph.D. degrees from the University of Colorado, Boulder, in 1991 and 1995, respectively.

From 1982 to 1988, he was a Design Engineer at Hyundai Engineering Co., Korea. Since 1996, he has been a Senior Member of R&D Staff at the Power Electronics Laboratory, Delta Products Corporation, Research Triangle Park, NC, the U.S. subsidiary of Delta Electronics, Inc., Taiwan, R.O.C. He holds 21 U.S. patents.

Dr. Jang received the IEEE TRANSACTIONS ON POWER ELECTRONICS Prize paper award for best paper published in 1996.

Milan M. Jovanović (F’01) received the Dipl. Ing. degree in electrical engineering from the University of Belgrade, Serbia.

Presently, he is the Chief Technology Officer of the Power Systems Business Group of Delta Electronics, Inc., Taipei, Taiwan, R.O.C. 

Dr. Jang received the EEE TRANSACTIONS ON POWER ELECTRONICS Prize paper award for best paper published in 1996.