1. Introduction

Recently, high power density has become one of the major requirements in today’s off-line power converters for computer–network servers and telecom equipment primarily due to a continuous growth in their system power needs. Some projections put the expected annual growth of power density of off-line power supplies at 10–15%. Specifically, in the near future, multiple-output ac/dc server power supplies are expected to attain power densities of over 7–10 W/in³, whereas ac/dc front-end power supplies for distributed power systems (DPSs) employed in high-end servers and telecom applications to generate a 12-V, 24-V, or 48-V dc-bus voltage are expected to exhibit power densities in the 15–20 W/in³ range. This already challenging task of continuous power-density improvements is further compounded by low profile (height) requirements of today’s server/telecom ac/dc power supplies, which adversely affects the optimal selection of some power components. Typically, the profile of today’s state-of-the-art server/telecom power supplies is 1U or 2U, where the height of 1U (unit) is equal to 1.75 inches.

Generally, to achieve the expected power densities, it is necessary to optimize power-stage performance and use advanced packaging/thermal management techniques. Namely, the power-stage performance optimization requires the employment of efficient high-frequency topologies that can reduce the size of the power stage.
without sacrificing its efficiency. This typically requires a soft-switching topology with optimized magnetic and semiconductor components so that the switching and conduction losses are kept at a minimum. However, an efficient power stage alone is not sufficient to bring about a significant power-density improvement. In fact, in today’s ac/dc power supply, the major opportunity for substantial power-density increases lays in the replacement of old, conventional packaging and thermal management techniques with new ones that would employ high-level component integrations, as well as new and more suitable materials. Currently, the packaging and thermal issues have been addressed in depth by researchers at National Science Foundation’s Center for Power Electronics Systems (CPES) at Virginia Tech.²⁻⁴ This paper does not deal with packaging and thermal management issues and techniques, but only with electrical circuit design issues related to high-power-density server power supplies.

As shown in Fig. 1, a typical ac/dc server power supply power stage consists of four major functional parts that require a significant volume. Specifically, the EMI filter, power-factor-correction (PFC) circuit, hold-up time energy-storage capacitor(s), and dc/dc output stage are integral parts of every ac/dc server power supply. The telecom ac/dc power supplies have the same structure except that the energy-storage capacitor(s) is sized based on the PFC circuit output ripple rather than based on the hold-up time specifications. To increase the power density, it is necessary to optimize the performance and minimize the size of all four parts since a partial optimization is insufficient to meet the future power-density requirements.

In this paper, circuit technologies and design optimization techniques suitable for high-density ac/dc server/telecom power supplies are reviewed. Specifically, technologies for high-performance PFC and dc/dc circuits, as well as techniques for hold-up time capacitor minimization, are discussed in details. Due to the absence of a practical EMI-filter design procedure, which is direct result of a lack of a systematic research effort in the EMI optimization area, the major EMI design issues are only briefly addressed. In addition, the focus of the present paper is on technologies for single-output ac/dc power supplies that are used as front ends in high-end server/telecom DPSs, i.e., on power-supplies with a 48-V or 12-V single output, which are expected to exhibit power densities over 15 W/in³.
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2. PFC Technologies

At higher power levels, the continuous-conduction-mode (CCM) boost converter is the preferred topology for implementation of a front-end with active input-current shaping. As a result, in recent years, significant efforts have been made to improve the performance of high-power boost converters. The majority of these development efforts have been focused on reducing the adverse effects of the reverse-recovery characteristic of the boost rectifier on the conversion efficiency and electromagnetic compatibility (EMC).

Generally, the reduction of reverse-recovery-related losses and EMC problems requires that the boost rectifier be “softly” switched off by controlling the turn-off rate of its current. So far, a number of soft-switched boost converters and their variations have been proposed. All of them use additional components to form a passive snubber, or an active snubber circuit that controls the turn-off $di/dt$ rate of the boost rectifier. Generally, the passive snubber approaches use only passive components such as resistors, capacitors, inductors, and rectifiers, whereas active snubber approaches also employ active switch(es).

Although passive lossless snubbers can improve efficiency, their performance is not good enough to make them viable candidates for applications in high-performance PFC circuits. Namely, the reported efficiency improvements for various passive lossless snubbers is in the 1–2% range depending on the line and load conditions, switching frequency, and boost rectifier characteristic. However, they suffer from increased component stresses and are not able to operate with soft switching of the boost switch, which is detrimental in high-density applications that require increased switching frequencies.

The simultaneous reduction of the reverse-recovery losses and soft switching can be achieved by active snubbers. As an example, Fig. 2 shows a boost converter

![Diagram of Boost PFC power stage with active snubber](image-url)
with an active snubber that employs a snubber inductor connected to the common node of the boost switch and the rectifier to control the turn-off rate of the rectifier current.\textsuperscript{12,13} In the circuit in Fig. 2, boost switch $S$ turns on with zero voltage switching (ZVS) and rectifier $D$ turns off under soft switching conditions. However, auxiliary switch $S_1$ is turned on while its voltage is equal to the output voltage, and subsequently turned off while carrying a current greater than the input current. Although it is switched under “hard” switching conditions, the power dissipation of the auxiliary switch in a properly designed converter is much smaller than that of the main switch because the auxiliary switch conducts only during switching transitions. The major drawback of the soft-switched converter in Fig. 2 is the undesirable resonance of output capacitance $C_{OSS1}$ of the auxiliary switch (not shown in Fig. 2) and snubber inductor $L_R$ that occurs when auxiliary switch $S_1$ is opened and after the current in $L_R$ falls to zero. This parasitic resonance generates an undesirable current through $L_R$, which increases the conduction losses and upsets the normal operation of the circuit. To reduce the effect of this resonance, it is necessary to add a rectifier and a saturable inductor in series with $L_R$,\textsuperscript{13} which somewhat degrades the conversion efficiency and increases the component count and cost of the circuit.

The performance of the circuit in Fig. 2 can be improved by implementing an active snubber with soft switching of the auxiliary switch. Figure 3 shows the implementation of the active snubber that beside ZVS of the main switch and soft switching of the boost rectifier, offers zero current switching (ZCS) of the auxiliary switch.\textsuperscript{14} Another implementation of the active snubber that offers ZVS of the main switch and ZCS of the auxiliary switch is shown in Fig. 4.\textsuperscript{15} In both implementations, a transformer, connected to the output of the boost converter, is used to provide voltage across resonant inductor $L_R$ to decrease the current through $L_R$.

![Fig. 3. Boost PFC power stage with active snubber.\textsuperscript{14}](image-url)
the inductor and, therefore, auxiliary switch $S_1$, down to zero before the switched is turned off. The circuits in Figs. 3 and 4 are expected to show similar performance.

Soft switching of all semiconductor components can also be achieved by employing an active snubber implemented with snubber inductor $L_s$ in series with main switch $S$ and rectifier $D$, as shown in Figs. 5 and 6.\footnote{16, 17} Both circuits offer ZVS turn-on of the main and the auxiliary switches, and ZVS turn-off of the rectifier. In addition, the circuits in Figs. 5 and 6 do not suffer from parasitic resonance, and, therefore, do not require additional components. However, the voltage stress of the main switch in these implementations is higher than that in the circuits in Figs. 2 through 4 because of the placement of the snubber inductor in series with the main switch and the rectifier. Nevertheless this increased voltage stress can be minimized by a proper selection of circuit components and the switching frequency.\footnote{16–18}
The difference between the implementations in Figs. 5 and 6 is in the point of connection of the active snubber consisting of a series connection of auxiliary switch \( S_1 \) and clamp capacitor \( C_C \). In the circuit in Fig. 5, the active snubber is connected to the anode of rectifier \( D \), whereas in the circuit in Fig. 6 it is connected to the cathode of rectifier \( D \). As a result, the circuits have different current waveforms through the components and require different timing of the drive signals for the main and auxiliary switches. Specifically, the circuit in Fig. 5 requires a more desirable overlapping gate drive, whereas the circuit in Fig. 6 requires a nonoverlapping gate drive that is, generally, more susceptible to noise than an overlapping gate drive. It should be noted that both circuits require a high-side driver for the auxiliary switch. However, the circuit in Fig. 6 can be implemented with an isolated active snubber, which has both the main and the auxiliary switches referenced to ground so that a direct (low-side), more desirable drive can be used for both switches.\(^\text{19}\)

Due to ZVS of the boost switch, the efficiency of the circuits in Refs. 12–19 was shown to be significantly improved when the boost switch is implemented with a MOSFET (metal-oxide-semiconductor field-effect transistor) device. Generally, the circuits in Fig. 2 through 6 improve the low-line conversion efficiency of a universal-line boost PFC for approximately 3–4\%\(^\text{12–19}\). However, the improvement in the efficiency of these circuits when used with an IGBT (insulate-gate bipolar transistor) device is expected to be much less because for IGBT devices zero-current switching (ZCS) is the optimal switching strategy.\(^\text{20}\)

A ZCS boost converter suitable for applications with IGBTs was introduced in Ref. 21. Although in this circuit the boost switch is turned off with zero current, the circuit exhibits an undesirable resonance between the snubber inductor and the output capacitance of the switches, which requires additional clamp and/or snubber circuits.\(^\text{22}\) The required clamp and snubber circuits not only increase the complexity and cost of the circuit, but also have a detrimental effect on its efficiency.

A soft-switching technique which is suitable for IGBT applications, and which does not suffer from undesirable resonance of circuit’s components, was introduced
in Ref. 23. This technique improves the performance of the PFC boost converter by eliminating the switching losses with a new zero-current-zero-voltage-switched (ZC-ZVS) active-snubber circuit that consists of a snubber inductor, a clamp diode, a clamp capacitor, and an auxiliary switch, as shown in Fig. 7. The ZC-ZVS snubber reduces the reverse-recovery-related losses of the rectifier and also provides soft switching of the main and auxiliary switches. Specifically, the main switch turns off with ZCS, whereas the auxiliary switch turns on with ZVS. In addition, because the proper operation of the ZC-ZVS snubber circuit requires that the conduction period of the main and the auxiliary switches overlap, the circuit in Fig. 7 is not susceptible to failures due to accidental overlapping of the main and auxiliary switch gate drives. Furthermore, the complexity and cost of the converter are further reduced because the converter requires simple nonisolated gate drives for both switches.

Finally, it should be noted that the recent advancements in the development of silicon carbide (SiC) rectifiers that have made SiC rectifiers commercially available are dramatically changing the boost converter design-optimization priorities. Since SiC rectifiers virtually have no reverse-recovery charge, the reverse-recovery related losses are not an issue and, consequently, a snubber circuit that controls the turn-off rate of the rectifier current is not needed anymore. In fact, SiC technology makes it feasible to dramatically increase the switching frequency of the boost converter and, eventually, reduce the size of the circuit, primarily the size of the boost inductor. However, the dramatic increase of the switching frequency without a deterioration of efficiency is only possible if the boost switch is soft-switched. As a result, a high-frequency boost PFC with a SiC rectifier still requires additional circuitry which is employed to create soft-switching conditions. Therefore, for PFCs with SiC rectifiers, the optimization focus is shifted from the reduction of rectifier switching losses to the minimization of switching losses of the boost switch. This optimization shift is likely to bring about a variety of new implementations of soft-switched boost PFC circuits.
3. Technologies for DC/DC Output Stage

The soft-switched, full-bridge (FB) PWM converter shown in Fig. 8 is the most widely used circuit in front-end ac/dc power supplies for server and telecom DPSs. This converter features ZVS of the primary switches with a relatively small circulating energy and at a constant switching frequency. The control of the output voltage at a constant frequency is achieved by the phase-shift technique. In this technique, the turn-on of a switch in the \( Q_3 \)-\( Q_4 \) leg of the bridge is delayed, i.e., phase-shifted, with respect to the turn-on instant of the corresponding switch in the \( Q_1 \)-\( Q_2 \) leg. The ZVS of the lagging-leg switches \( Q_3 \) and \( Q_4 \) is achieved primarily by the energy stored in output filter inductor \( L_F \). Since the inductance of \( L_F \) is relatively large, the energy stored in \( L_F \) is sufficient to discharge output parasitic capacitance \( C_3 \) and \( C_4 \) of switches \( Q_3 \) and \( Q_4 \) in the lagging-leg and to achieve ZVS even at very light load currents. However, the discharge of parasitic capacitance \( C_1 \) and \( C_2 \) of leading-leg switches \( Q_1 \) and \( Q_2 \) is done by the energy stored in leakage inductance \( L_{LK} \) of the transformer because during the switching of \( Q_1 \) or \( Q_2 \), the transformer primary is shorted by the simultaneous conduction of rectifiers \( D_1 \) and \( D_2 \) that carry the output filter inductor current. Since leakage inductance \( L_{LK} \) is
small, the energy stored in $L_{LK}$ is also small so that ZVS of $Q_1$ and $Q_2$ cannot be achieved even at relatively high output currents. The ZVS range of the leading-leg switches can be extended to lower load currents by intentionally increasing the leakage inductance of the transformer and/or by adding a large external inductance in series with the primary of the transformer. If properly sized, the external inductance can store enough energy to achieve ZVS of the leading-leg switches even at very low currents. However, a large external inductance also stores extremely high energy at full load that produces a large circulating energy, which adversely affects the stress of the semiconductor components and the conversion efficiency. In addition, a large inductance in series with the primary winding (leakage inductance and/or external inductance) reduces the effective duty cycle on the secondary side because it extends the time required to change polarity of the primary current. To make up for the reduced duty cycle, the turns ratio of the transformer must be reduced, which has detrimental effect on the performance because of increased component losses and stresses.\(^{27}\)

Another major limitations of the circuit in Fig. 8 is the severe parasitic ringing at the secondary of the transformer during the turn-off of a rectifier caused by the resonance of the rectifier's junction capacitance with the leakage inductance of the transformer and/or the external inductance. To control the ringing, a heavy snubber circuit needs to be used on the secondary side, which may significantly lower the conversion efficiency of the circuit.\(^{28}\) In fact, the loss of duty cycle and secondary-side parasitic ringing are the major factors that limit the maximum switching frequency of kilowatt-range FB ZVS-PWM circuits to around 100 kHz.\(^{29}\)

The ZVS range of the leading-leg switches in the FB ZVS-PWM converter in Fig. 8 can be extended to lower load currents without a significant increase of the circulating energy by using a saturable external inductor instead of a linear inductor.\(^{29}\) If the saturable inductor is designed so that it saturates at higher load currents, it will not store excessive energy at high loads. At the same time, at low load currents when the inductor is not saturated, it will have a sufficiently high inductance to store enough energy to provide ZVS of the leading-leg switches even at very light loads. While it was demonstrated that a properly designed saturable inductor can improve the performance of the FB ZVS-PWM converter, the circuit requires a relatively large-size magnetic core to implement the inductor, which increases the cost of the circuit. Generally, a larger core is required to eliminate the thermal problem that is created by excessive core loss because the saturable core is placed in the primary circuit and its flux swings between the positive and negative saturation levels.

The ZVS range of the FB ZVS-PWM converter can also be extended to lower load currents by placing saturable cores on the secondary side, as shown in Fig. 9. Since in the implementation in Fig. 9, saturable cores $L_{SAT1}$ and $L_{SAT2}$ are connected in series with rectifiers $D_1$ and $D_2$, their flux swing is confined between zero and the positive saturation level, i.e., it is a half of the flux swing of the saturable core in Fig. 9. As a result, the total core loss in the circuit in Fig. 9 is reduced
compared to that of the circuit in Fig. 8. However, because in voltage step-down converters (i.e., converters with output voltage $V_O$ smaller than input voltage $V_{IN}$), secondary currents are larger than the primary current, the total copper loss of the saturable core windings in Fig. 9 is increased compared to the corresponding loss in the circuit in Fig. 8. An additional feature of secondary-side saturable inductors $L_{SAT1}$ and $L_{SAT2}$ is that they serve as turn-off snubbers for rectifiers $D_1$ and $D_2$, damping the parasitic oscillations between the junction capacitance of the rectifiers and the leakage inductance of the transformer, as well as helping to reduce the reverse-recovery current losses if fast-rectifier rectifiers are used.

The FB ZVS-PWM with secondary-side saturable inductors can be implemented with or without freewheeling rectifier $D_{FW}$, which is shown with dashed lines in Fig. 9. The operation of the circuit in Fig. 9 with freewheeling diode $D_{FW}$ is identical to that with the saturable inductor on the primary side. Namely, with $D_{FW}$, saturable inductors $L_{SAT1}$ and $L_{SAT2}$ are used to store enough energy at lower load currents so that ZVS of the primary switches is achieved with minimum circulating energy. However, in the implementation without freewheeling diode $D_{FW}$, saturable inductors $L_{SAT1}$ and $L_{SAT2}$ are not used for energy storage. Instead, they are used to briefly delay the conduction of the nonconducting rectifier after a switch in a bridge leg is turned off and, consequently, force the current through filter inductor.
$L_F$ to continue to flow through the rectifier which already has been conducting. As a result, in the implementation of the circuit in Fig. 9 without freewheeling rectifier $D_{FW}$, the energy stored in output filter inductor $L_F$ is used to create ZVS condition for leading-leg switches $Q_1$ and $Q_2$ in the same way as it is used to create ZVS conditions for switches $Q_3$ and $Q_4$ in the lagging-leg, i.e., by utilizing the energy stored in output-filter inductor $L_F$.

An approach that deals with the secondary-side ringing problem in a simple and effective way was introduced in Ref. 32. In this approach, shown in Fig. 10, the secondary-side ringing due to the resonance of the capacitance of the secondary-side rectifier and external primary inductor that is employed to extend the ZVS range is controlled by primary-side clamp diodes $D_{C1}$ and $D_{C2}$. If the leakage inductance of the transformer is minimized, the primary clamp circuit also effectively clamps the voltage across the secondary winding so that parasitic ringing and its associated voltage stress are virtually eliminated. Due to its simplicity, the circuit in Fig. 10 has found use in many applications, particularly, in high-power switch-mode rectifiers (SMRs) employed in telecommunication power systems. However, the circuit in Fig. 10 does not offer any reduction of the secondary-side duty-cycle loss, or circulating energy.

A number of techniques that can achieve ZVS of all primary switches in the entire input-voltage and load range virtually without a loss of duty cycle and

\[ \text{Fig. 10. FB ZVS-PWM converter with primary-side clamp diodes.}^{32} \]
secondary-side ringing have been proposed in Refs. 33–36. Generally, these circuits achieve ZVS of all primary switches in the entire load and input-voltage range by utilizing energy stored in inductive components of an auxiliary circuit. In the approach described and analyzed in Refs. 33 and 34, the auxiliary circuit comprises a pair of inductors that connected between the mid-point of the bridge legs and a mid-point of an input-voltage capacitive divider, whereas in the approach described in Ref. 35, the energy stored in a magnetizing inductance of an auxiliary transformer is used to extend the ZVS range. While in the FB ZVS-PWM converters described in Refs. 33–35, the energy available for ZVS increases as the input-voltage increases, which is the desirable direction of change since more energy is required to achieve ZVS at higher input voltages, the stored energy in these FB ZVS converters is independent of load. As a result, they cannot optimally resolve the trade-off between power-loss savings brought about by a full-load-range ZVS and power losses of the auxiliary circuit. Ideally, the auxiliary circuit needs to provide very little energy, if any, at full load since the full-load current stores enough energy in converter’s inductive components to achieve a complete ZVS of all switches. As the load current decreases, the auxiliary circuit needs to provide progressively more ZVS energy, with the maximum energy required at no load. A FB ZVS-PWM converter that features this kind of adaptive energy storage in the auxiliary circuit has been introduced in Ref. 36.

This converter, shown in Fig. 11, employs a primary-side coupled inductor connected between the bridge legs to achieve a wide-range ZVS. Generally, the secondary-side of the circuit in Fig. 11 can be implemented with any type of the full-wave rectifier such as the full-wave rectifier with a center-tapped secondary, the full-wave rectifier with current doubler, or the full-bridge full-wave rectifier. However, in high-power applications, the current-doubler rectifier shown in Fig. 11 is usually used since it shows the best performance. The control of the circuit in Fig. 11 is the same as the control of any other constant-frequency FB ZVS converter, i.e., any of the integrated phase-shift controllers available on the market can be used.

In the circuit in Fig. 11, the ZVS of leading-leg switches $Q_3$ and $Q_4$ is achieved primarily by the energy stored in the magnetizing inductance of coupled inductor $L_C$, whereas the ZVS of the lagging-leg switches $Q_1$ and $Q_2$ is achieved by the sum of the energy stored in the magnetizing inductance of $L_C$ and output filter inductance $L_F$. By properly selecting the value of the magnetizing inductance of the coupled inductor, all primary switches in the converter in Fig. 11 can achieve ZVS even at no load. Because in the circuit in Fig. 11 the energy required to create ZVS conditions at light loads does not need to be stored in the leakage inductance, the transformer leakage inductance can be minimized. As a result, the loss of the duty cycle on the secondary-side is minimized, which maximizes the turns ratio of the transformer and, consequently, minimizes the conduction losses. In addition, the minimized leakage inductance of the transformer significantly reduces the secondary-side ringing caused by the resonance between the leakage inductance
and junction capacitance of the rectifier, which greatly reduces the power dissipation of a snubber circuit that is usually used to damp the residual high frequency ringing. For a properly selected maximum turns ratio of the transformer, the conduction loss of the converter in Fig. 11 can be reduced by as much as 30% compared to the corresponding loss in the conventional circuit in Fig. 8. Furthermore, because of the ZVS operation across the entire load and line range, the converter in Fig. 11 can efficiently operate even at significantly higher frequencies than the circuit in Fig. 8.

Generally, bridge-type topologies are not used in multiple output power supplies that are supposed to deliver high currents from low-voltage outputs. Instead, single-ended topologies are employed because they are more suitable for implementations with synchronous rectifiers (SRs) and mag-amp post regulators.\textsuperscript{39,40} The topology choices in these implementations are limited to the single-switch and two-switch forward converters and their variations. Their power density is primarily limited by a relatively low maximum frequency at which mag-amps can efficiently work. Typically, mag-amp performance rapidly deteriorates at frequencies above
the 100–150 kHz range. Therefore, to improve the power density, it is necessary to resort to implementations without mag-amps. This can be done either by system partitioning where the number of post-regulated outputs is reduced by the employment of multiple number of power stages (converters), or by the employment of dc/dc post regulators, or by their combination. As an example, 12-V, 5-V, and 3.3-V outputs can be generated by a converter that has a 12-V output and employs two dc/dc step-down converters to create the 5-V and 3.3-V outputs.

4. Techniques for Hold-Up-Time Energy-Storage Minimization

As the required power and power density of ac/dc datacom power supplies increase, the size of the hold-up-time energy-storage (bulk) capacitors, which store the energy that is used to deliver power to the load for a short time (typically 10–20 ms) after a line dropout, becomes a significant factor in limiting the maximum attainable power density. Therefore, the minimization of the hold-up-time capacitor size is an indispensable design step in maximizing the power density of ac/dc datacom power supplies. The minimization of the size of the hold-up-time capacitors can be accomplished by advancements in capacitor technology that would increase the volumetric efficiency (µF/in³) of the energy-storage capacitors and/or by circuit optimization techniques that would minimize the amount of capacitance needed for a given hold-up-time. In this paper, only the circuit techniques that can be used to minimize the energy-storage capacitors are discussed.

To achieve a desired hold-up-time, the dc/dc converter output stage must be designed to operate in a certain voltage range with minimum energy-storage-capacitor voltage \( V_{BMIN} \) lower than voltage \( V_{BH} \) that corresponds to the line voltage at which hold-up-time is defined, as illustrated in Fig. 12. With such a design of the dc/dc output stage, the energy storage capacitor delivers power to the output after a line dropout until the energy-storage-capacitor discharges to \( V_{BMIN} \).

Generally, for a given \( V_{BH} \) and \( V_{BMIN} \), larger power \( P_{OH} \) and/or longer hold-up-time \( T_H \) requires a larger energy-storage-capacitor \( C_B \). As a result, in high-power

![Energy-storage-capacitor voltage waveform during hold-up-time.](image-url)
applications, the size of energy-storage-capacitor(s) very often limits the maximum power density. To maximize power density, the size of energy-storage-capacitors must be minimized. A limited size reduction of energy-storage-capacitor $C_B$ can be achieved by extending the regulation range of the dc/dc converter output stage by minimizing voltage $V_{BMIN}$ at which the dc/dc converter output stage drops out of regulation. However, because of a strong trade-off between minimum regulation voltage $V_{BMIN}$ and the conversion efficiency of the dc/dc converter output stage, $V_{BMIN}$ is usually restricted to 80% to 90% of $V_{BH}$. With such a selection of $V_{BMIN}$, only a small part of the energy stored in $C_B$ is delivered during the hold-up-time period.

As illustrated in Fig. 13, which shows the percentage of the total stored energy delivered to the load during the hold-up-time as a function of selected $V_{BMIN}$, only 19% of the stored energy is delivered to the load during the hold-up-time if $V_{BMIN}$ is selected to be 0.9$V_{BH}$. Similarly, if $V_{BMIN} = 0.8V_{BH}$, 36% of the stored energy is delivered to the output, i.e., still the majority of the stored energy is not used to supply the load during the hold-up-time.

To utilize the majority of the stored energy during the hold-up-time, $V_{BMIN}$ must be selected well below 80% of $V_{BH}$. For example, 75% of the stored energy is delivered to the load for $V_{BMIN} = 0.5V_{BH}$. However, with $V_{BMIN} = 0.5V_{BH}$, the efficiency of the dc/dc converter and, therefore, the overall efficiency would be severely penalized because the dc/dc converter output stage would be required to operate with a much wider input voltage range. Namely, to regulate the output
in a wider input-voltage range, a wider duty-cycle range is needed, which dictates
the selection of a smaller turns ratio of the transformer. Generally, a smaller turns
ratio increases the primary and, very often, secondary conduction losses, which
deteriorates the conversion efficiency.

So far, two techniques for the minimization of the hold-up-time capacitor size
without the efficiency degradation are proposed and demonstrated. The technique
described in Ref. 41 employs variable transformer-turns-ratio concept, whereas in
the technique introduced in Ref. 42 employs a hold-up-time extension circuit to
maximize the utilization of the stored energy. The implementation of the variable-
turns-ratio circuit is shown in Fig. 14. In this circuit the effective turns ratio of
the transformer can be changed by secondary-side switch $Q$. Switch $Q$ is turned on
only during the hold-up-time period, otherwise switch $Q$ is off. When switch $Q$ is
off, windings $N_2$ are open so that the turns ratio is maximal at $n = \frac{N}{N_1}$, which
maximizes the conversion efficiency. During the hold-up-time mode of operation

Fig. 14. FB ZVS-PWM converter with variable turns-ratio transformer.\textsuperscript{41}
when switch $Q$ is on, windings $N_2$ conducts. As a result, the turns ratio of the transformer is reduced to $n = N/(N_1 + N_2)$, which allows the converter to operate down to a lower bulk capacitor voltage so that the utilization of the energy stored in the bulk capacitors is optimized. A potential problem of the circuit in Fig. 14 is a possible out-of-spec disturbance of the output-voltage caused by an abrupt change of the turns ratio of the transformer at the moment switch $Q$ is turned on. In addition, this concept is not suitable for applications in multiple-output power supplies because it would require a separate switch and windings for each output.

The conceptual block diagram of the hold-up-time extension circuit is shown in Fig. 15(a). Generally, the improved utilization of the stored hold-up-time energy is obtained by providing two energy storage capacitors, $C_{BO}$ and $C_{BAUX}$, and by connecting auxiliary energy-storage-capacitor $C_{BAUX}$ to the input of the hold-up-time extension circuit that has the output connected to the energy-storage-capacitor $C_{BO}$. To ensure proper operation, diodes $D_{BO}$ and $D_{BAUX}$ are used to provide necessary decoupling of certain parts of the circuits during different phases of operation. It should be noted that depending on the actual implementation of the front-end rectifier circuit, as well as the hold-up-time circuit, diode $D_{BAUX}$ may not be required.

Since the hold-up-time extension circuit is connected at the input of the dc/dc output stage, its performance and complexity is unaffected by the dc/dc output stage topology and number of outputs. In addition, since the hold-up-time extension circuit acts outside the control loop of the dc/dc output stage, the dc/dc output(s) are virtually immune to the disturbance that may be generated at the moment the hold-up-time extension circuit is activated.

The hold-up-time extension circuit is designed so that its output is regulated at voltage $V_{BAUX}$ that is lower than the normal-mode-operation voltage $V_{BH}$ and slightly higher than the minimum regulation voltage of the dc/dc converter $V_{BMIN}$. As a result, the hold-up-time extension circuit is inactive during the normal mode of operation, i.e., when the ac line is present at the input of the power supply. In fact, during the normal mode of operation, capacitors $C_{BO}$ and $C_{BAUX}$ are connected in parallel so that their voltages are equal if the voltage drop across rectifier $D_{BO}$ is neglected.

When the ac line drops out, the output power is first supplied by the energy stored in capacitors $C_{BO}$ and $C_{BAUX}$. As a result, the capacitors start discharging and their voltages starts decreasing, as shown in Fig. 15(b). During this phase of operation, voltage $V_{BO}$ across capacitor $C_{BO}$ and voltage $V_{BAUX}$ across capacitor $C_{BAUX}$ track each other since the capacitors are simultaneously discharging. In fact, the operation of the circuit during this phase is identical to that of the circuit without the hold-up-time extension circuit. When the voltage across the capacitors reaches a level close to the minimum regulation voltage of the dc/dc converter $V_{BMIN}$, i.e., when $V_{BO} = V_{BAUX} \approx V_{BMIN}$, the hold-up-time extension circuit becomes activated. Once the hold-up-time extension circuit is activated, the capacitor $C_{BAUX}$ connected to the input of the hold-up-time extension circuit continues to
discharge and provide energy to the regulated output of the hold-up-time extension circuit, which keeps the voltage across capacitor $C_{BO}$ constant at approximately $V_{BMIN}$, as shown in Fig. 15(b). Therefore, during this phase of operation, energy stored in capacitor $C_{BAUX}$ is used to delivered the required output power during the hold-up-time. The hold-up-time is terminated when the voltage across $C_{BAUX}$
decreases to $V_{BAUXMIN}$, which is the minimum regulation voltage of the hold-up-time extension circuit.

As can be seen from Fig. 15(b), the extension of the hold-up-time brought about by the hold-up-time extension circuit is dependent on the selection of $V_{BAUXMIN}$. A lower $V_{BAUXMIN}$ results in a longer extension of the hold-up-time because more energy is taken from capacitor $C_{BAUX}$. For a given $V_{BAUXMIN}$, the extension of the hold-up-time depends on the size of $C_{BAUX}$ and it increases as the capacitance of $C_{BAUX}$ is increased.

To evaluate the effectiveness of the proposed hold-up-time extension method, Fig. 16 shows plots of the ratio of the additional discharge energy due to the hold-up-time extension circuit $\Delta E_{CBEC}$ and the energy discharge without the hold-up extension circuit $\Delta E_{CB}$ as functions of $V_{BAUXMIN}/V_{BH}$ and for different $C_{BAUX}/(C_{BO} + C_{BAUX})$ ratios. The solid lines in Fig. 16 present plots for $V_{BMIN}/V_{BH} = 0.9$, whereas the dashed lines show plots for $V_{BMIN}/V_{BH} = 0.8$, i.e., for two regulation ranges of the dc/dc converter output stage. The plots are generated by assuming that $C_{BO} + C_{BAUX} = C_B$, i.e., that total energy storage capacitance in the implementations with and without the hold-up-time circuit is the same. Therefore, different ratios of $C_{BAUX}/C_B$ used as the parameter in the plots.

![Fig. 16. Plot of ratio of additional discharged energy due to hold-up-time extension circuit $\Delta E_{CBEC}$ and discharge energy without hold-up-time extension circuit $\Delta E_{CB}$ as functions of $C_{BAUX}/C_B$ and $V_{BAUXMIN}/V_{BH}$. Solid line for $V_{BAUXMIN}/V_{BH} = 0.9$, dashed line for $V_{BAUXMIN}/V_{BH} = 0.8$.](image-url)
in Fig. 16 mean different allocations of the total capacitance $C_B$ among auxiliary capacitance $C_{BAUX}$ and capacitance $C_{BO}$.

As can be seen from Fig. 16, for a given ratio $V_{BAUX_{MIN}}/V_{BH}$, the amount of extracted energy from the energy-storage capacitors is increased as the ratio $X = C_{BAUX}/C_B$ increases, i.e., as more of the total capacitance is allocated to $C_{BAUX}$. For example, for $V_{BMIN}/V_{BH} = 0.9$ (solid lines), $V_{BAUX_{MIN}}/V_{BH} = 0.5$, and $X = 0.25$, the hold-up-time extension circuit helps extract approximately 70% more energy from the energy-store capacitors compared with the implementation without the hold-up-time extension circuit that has the same amount of the energy-storage capacitance. For larger values of ratio $X = C_{AUX}/C_B$, the effect of the hold-up-time extension circuit is even more dramatic since it increases the amount of the delivered energy from the storage capacitors by approximately 150% and 220% for $X = 0.5$ and $X = 0.75$, respectively.

The effectiveness of the hold-up-time extension circuit is also dependent on the regulation range of the dc/dc converter, i.e., it is dependent on the $V_{BMIN}/V_{BH}$ ratio. As can be seen from Fig. 16, for $V_{BMIN}/V_{BH} = 0.8$ (dashed lines) and $V_{BAUX_{MIN}}/V_{BH} = 0.5$, the hold-up-time extension circuit helps extract approximately 25%, 55%, and 80% more energy for $X = 0.25$, $X = 0.5$, and $X = 0.75$, respectively. Generally, for the maximum effectiveness of the hold-up-time circuit, it is necessary to maximize auxiliary capacitance $C_{BAUX}$ since the energy stored in this $C_{BAUX}$ is delivered to the output when the hold-up-time extension circuit is activated. The energy stored in capacitor $C_{BO}$ is only delivered during the hold-up-time period before the hold-up-time extension circuit is activated at approximately $V_{BMIN}$. Therefore, the design optimization of the hold-up-time extension circuit requires that the available total energy-storage capacitance be allocated between $C_{BO}$ and $C_{BAUX}$ so that $C_{BAUX}$ is maximized. In practice, this allocation is usually dictated by the minimum capacitance $C_{BO}$ that can handle the voltage and current ripple produced at the output of the hold-up-time extension circuit.

Because when the hold-up-time extension circuit is activated the voltage across $C_{BAUX}$ is lower than the voltage across $C_{BO}$, as shown in Fig. 15(b), the hold-up-time extension circuit can be implemented with any boost-like nonisolated or isolated topology. Figure 17 shows the implementation of the hold-up-time extension circuit with the boost topology.

5. EMI Filter Optimization Issues

In today’s power supplies, the size and power loss of the EMI filter is emerging as one of the major limitations to further power-density and efficiency improvements. The primary reason is the lack of practical design techniques for size and loss optimization, although a number of useful papers addressing various EMI measurement, simulation, and component-value selection issues have been published in recent years.43–48 As a result, the cut-and-try method is still the prevalent design optimization technique used today in the power supply industry.
Generally, to minimize the size of an EMI filter, it is not only necessary to minimize the number of the filter stages by careful design of the circuit layout and selection of filter component values, but also it is necessary to develop fabrication/packaging techniques that would minimize the size of filter’s magnetic components such as differential and common-mode filters. Whereas component-value optimization issues are being slowly but surely addressed, size optimization issues are still waiting to get their due attention.

Typically, the dominant loss in EMI filters for high-power power supplies is the copper loss of the windings of the differential and common-mode chokes. Therefore, one of the major tasks in the optimization of the EMI filter performance and size is to maximize the amount of copper so that the copper loss is reduced and conversion efficiency maximized. The second task is to find efficient thermal-management and packaging methods to extract the residual heat out of the filter, which would allow for a further filter-size reduction.

Finally, the size of the capacitive components of an EMI filter such as $X$ and $Y$ capacitors, which may become a power-density limiting factor once the size of filter’s magnetic components is optimized, must be also reduced. While some reduction of the $X$ and $Y$ caps can be gained through filter optimization, a major size reduction is expected from the advancements in the capacitor technology. Perhaps, the future
generation X and Y caps for use in high-power density EMI filters will be of a surface-mounted type.

6. Summary

Ever-increasing power density requirements of modern ac/dc server and telecom power supplies pose a formidable challenge to power supply designers. To succeed in meeting these high-power density requirements, it is necessary to optimize performance and size of all major functional parts of the power supply. Specifically, the utmost attention needs to be paid to the performance and size optimizations of the PFC front-end converter, dc/dc output stage, and EMI filter, as well to the size optimization of the hold-up-time energy-storage capacitors.

While circuit optimization is certainly an indispensable ingredient in increasing power density, the major future power-density gains are expected from advancements in thermal management and packaging technologies that will enable higher component integration levels. In addition, advancements in active and passive component technologies such as new materials and packaging solutions will play a major role in a continuous push for ever-higher power densities.

With the recent introduction of the SiC (Silicon Carbide) technology, which makes it feasible to operate existing converters at significantly higher switching frequencies, the bottleneck for size reduction is shifting from semiconductor devices to passive components. In fact, at high switching frequencies, increased core and winding losses in magnetic components and the volume required for the hold-up-time energy-storage capacitors are emerging as the major factors that limit the maximum attainable power density.

References

7. M. M. Jovanović, Z. Chen and P. Liao, Evaluation of active and passive snubber techniques for applications in power-factor-correction boost converters, *Sixth Int. Conf.*


