Abstract—In this paper, a systematic review of phase-locked loop (PLL)-based closed-loop control methods for interleaved discontinuous conduction mode/continuous conduction mode (DCM/CCM) boundary boost power factor correction (PFC) converters is presented. A detailed analysis of the stability of the PLL with instant averaging filter is performed and verified by simulation. The stability of the PLL with instant averaging filter and with RC filter is compared by simulation. Based on the simulation results, it is concluded that the PLL-based closed-loop methods always provide stable operation, unlike the open-loop control methods, where the only method that results in stable operation is the slave synchronization to the turn-ON instant of the master with current-mode control. It is also shown that the dynamic response of the PLL-based closed-loop methods with master–slave approach and democratic approach is almost identical. Experimental results obtained based on a 300-W, universal input, 400-V output, interleaved DCM/CCM boundary boost PFC prototype circuit with a dedicated controller IC utilizing a democratic, PLL-based closed-loop method are also provided.

Index Terms—Closed-loop control, discontinuous conduction mode (DCM)/continuous conduction mode (CCM) boundary, interleaved boost converter, phase-locked loop (PLL), power factor correction (PFC), single-phase rectifier.

I. INTRODUCTION

In OFF-LINE power supplies that require active power factor correction (PFC), a boost converter operating at the boundary of discontinuous conduction mode (DCM) and continuous conduction mode (CCM) is a widely employed topology at low power levels (up to 200–300 W) [1]–[5]. The major benefit of the DCM/CCM boundary boost PFC converter, compared to the CCM boost PFC converter, is that the reverse-recovery losses of the boost diode are eliminated [6]. In addition, turn-ON with zero-voltage switching (ZVS) of the boost switch or near ZVS (also called valley switching) can be easily achieved. Other benefits of the DCM/CCM boundary boost PFC converter compared to the constant-switching-frequency DCM boost PFC converter are a lower total harmonic distortion (THD) of the line current, and a smaller peak inductor current resulting in lower turn-OFF switching losses and lower conduction losses [7]. Although the DCM/CCM boundary boost PFC converter exhibits a smaller peak inductor current than the DCM boost PFC converter, its peak inductor current is still twice its average current, which often necessitates a large differential mode (DM) electromagnetic interference (EMI) filter [10]. Another drawback is that its switching frequency, which changes with the instantaneous line voltage and the output power, varies over a wide range [4], [5]. Generally, the input current ripple and, consequently, the input DM–EMI filter can be significantly reduced by interleaving two or more boost PFC converters as shown in Fig. 1 [8]–[23]. In addition, the output current ripple can also be significantly reduced, resulting in a reduced equivalent-series-resistance (esr) loss of the output capacitor and, possibly, a reduction in capacitor volume. Another benefit of interleaving is that the efficiency at lighter loads can be increased by employing phase shedding, i.e., by progressively turning off converters as the load is decreased.

By interleaving two or more DCM/CCM boundary boost converters, the benefits of DCM/CCM boundary boost PFC converters mentioned earlier can be extended to higher power levels. However, since the switching frequency is variable, the synchronization of interleaved DCM/CCM boundary boost PFC converters presents a challenging task.

Very few implementations of the interleaved DCM/CCM boundary boost PFC converters have been published in the literature [10]–[23]. All of the previously published implementations except one [22] are based on a master–slave relationship, where the master converter operates as a stand-alone converter, whereas the slave converter is partially controlled by the master in order to achieve proper interleaving, i.e., a proper phase shift with respect to the master. It has been shown that the slave converter can be synchronized to the master converter

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with an open-loop method [10]–[15], i.e., by generating a time delay equal to half the switching period of the master determined from its previous switching cycle, or with a closed-loop method [16]–[18], [23], i.e., by measuring the phase difference between the converters and adjusting the phase of the slave based on the phase error. The slave converter with open-loop synchronization can be synchronized to the turn-ON instant of the master converter [11]–[14] or to the turn-OFF instant of the master converter [10], [15]. In both cases, the converters can operate either with current-mode control or with voltage-mode control. A detailed analysis of the open-loop synchronization methods of the slave converter to the master converter is presented in [19]. It is shown in [19] that among the open-loop synchronization methods, only the method when the slave is synchronized to the turn-ON instant of the master with current-mode control can provide a stable operation. The slave converter with closed-loop synchronization has been synchronized to the master converter by using a phase-locked-loop (PLL) approach. The PLL approach has been implemented by using a conventional low-pass filter [16]–[18] or a cycle-by-cycle instant averaging filter [23], and then adjusting the turn-OFF instant of the slave converter. Although PLL-based closed-loop methods where the turn-ON instant of the converter(s) is adjusted can be implemented, they are, generally, not attractive because of the additional complexity needed to achieve valley switching. Instead of the master–slave PLL interleaving, a democratic PLL interleaving is employed in [22], where the turn-OFF instant of both converters is adjusted proportionally to the phase error. In fact, in [22], the phase shift between the two converters is measured the same way as in the master–slave PLL method. However, unlike the master–slave method, where only the slave’s turn-OFF instant is adjusted, in the democratic method, the turn-OFF instant of both converters is adjusted in equal but opposite directions.

In this paper, a systematic review of the PLL-based closed-loop control methods for interleaved DCM/CCM boundary boost PFC converters is presented. A small-signal model of the PLL with instant averaging filter is developed and verified by simulation. The stability of the PLL with instant averaging filter and RC filter is demonstrated by simulation in both frequency and time domain. Based on the simulation results, it is concluded that the PLL-based closed-loop methods always provide stable operation. The dynamic response of the PLL-based closed-loop methods with master–slave approach and democratic approach is compared using simulations, and it is shown that their dynamic response is almost identical. Experimental results obtained on a 300-W, universal input, 400-V output, interleaved DCM/CCM boundary boost PFC prototype circuit with a dedicated controller IC utilizing a democratic PLL-based closed-loop method are also provided.

II. REVIEW OF PLL-BASED CLOSED-LOOP INTERLEAVING METHODS

The block diagram and key waveforms of the PLL-based control circuit with master–slave approach of two interleaved DCM/CCM boundary boost PFC converters are presented in Figs. 2 and 3, respectively. The phase difference between the gate-drive signals of the master and slave converters is sensed by a positive-edge-triggered SR flip-flop. The output voltage of the SR flip-flop $v_{\Delta \phi}$ is averaged by a low-pass filter, which can be implemented by using either a simple RC filter or a cycle-by-cycle instant averaging filter. For simplicity, cycle-by-cycle instant averaging of voltage $v_{\Delta \phi}$ is shown in Fig. 3, where the averaged voltage $v_{\Delta \phi, av}$ is constant over a switching cycle. The averaged voltage $v_{\Delta \phi, av}$ is compared to a reference voltage $(V_{CC}/2)$ that corresponds to the desired phase difference of 180° between the gate-drive signals of the master and slave converters. The phase-error voltage $v_{\Delta \phi, error}$ is used to adjust the turn-OFF instant of the slave converter.

When the phase shift of the slave’s gate signal with respect to the master’s gate signal is 180°, i.e., $T_{\Delta \phi} = T_{sw}/2$, the phase error voltage $v_{\Delta \phi, error} = 0$ (solid lines in Fig. 3). When $T_{\Delta \phi} > T_{sw}/2$, $v_{\Delta \phi, error} > 0$ (dashed lines in Fig. 3), while when $T_{\Delta \phi} < T_{sw}/2$, $v_{\Delta \phi, error} < 0$.

Both the master and slave converters can operate either with voltage-mode or current-mode control. In both control methods, the turn-OFF instant of the slave converter can be adjusted either by modifying the level of the slave’s feedback error voltage or by modifying the slope of the slave’s ramp signal, as illustrated in Fig. 4. It should be noted that both the master and slave converters turn on with valley switching after zero-current detection (ZCD) of their respective inductor currents.
Fig. 4. Adjustment of turn-OFF instant of slave converter by modifying the level of slave’s feedback error voltage when operating with (a) current-mode control, (b) voltage-mode control, or by modifying the slope of slave’s ramp signal when operating with (c) current-mode control, and (d) voltage-mode control.

An implementation of the PLL-based control circuit with master–slave approach of two interleaved DCM/CCM boundary boost PFC converters is shown in Figs. 5 and 6, respectively.

In Fig. 5, the slave’s feedback error voltage is obtained as

\[ V_{FBerrorS} = V_{FBerror} + \Delta V_{FBerrorS} \]  

where the adjustment voltage is

\[ \Delta V_{FBerrorS} = R_2 i_{\Delta \phi error} \]  

Assuming that \( Q_1 - Q_4 \) have identical characteristics, the phase-error current \( i_{\Delta \phi error} \) is proportional to the phase-error voltage \( v_{\Delta \phi error} \), i.e.

\[ i_{\Delta \phi error} = -\frac{2}{R_1} v_{\Delta \phi error} \]  

Substituting (3) in (2), the adjustment of the slave’s feedback error voltage is obtained as

\[ \Delta V_{FBerrorS} = -\frac{2R_2}{R_1} v_{\Delta \phi error} \]  

When \( T_{\Delta \phi} > T_{sw}/2 \), \( v_{\Delta \phi error} > 0 \), and \( i_{\Delta \phi error} < 0 \), resulting in a reduced level of the slave’s feedback error voltage and, consequently, in a reduced ON-time of the slave converter and a reduced phase shift of the slave’s gate signal with respect to the master’s gate signal, as shown in Fig. 3.

In Fig. 6, the slope of the slave’s voltage ramp is obtained as

\[ \frac{dv_{rampS}}{dt} = \frac{I_{rampS}}{C_{rampS}} + \frac{i_{\Delta \phi error}}{C_{rampS}} \]  

where the phase error current \( i_{\Delta \phi error} \) is defined by (3). However, the phase-error voltage \( v_{\Delta \phi error} \) in Fig. 6 has an opposite sign compared to that in Fig. 5 because in Fig. 6 the input of the low-pass filter is connected to the \( \bar{Q} \) output of the SR flip-flop. Therefore, when \( T_{\Delta \phi} > T_{sw}/2 \), \( v_{\Delta \phi error} < 0 \) and \( i_{\Delta \phi error} > 0 \), resulting in an increased slope of the slave’s voltage ramp and, consequently, again in a reduced ON-time of the slave converter and a reduced phase shift of the slave’s gate signal with respect to the master’s gate signal.

It should be noted that the implementation of the PLL-based control circuit in Fig. 5 is applicable for both voltage-mode and current-mode control, whereas, Fig. 6 illustrates a voltage-mode implementation. A simplified current-mode implementation corresponding to Fig. 6 is presented in Fig. 14.

The block diagram of the PLL-based control circuit with democratic approach of two interleaved DCM/CCM boundary boost PFC converters is presented in Fig. 7. The key difference between the master–slave and democratic approaches is that the...
phase-error voltage \( v_{\Delta \text{error}} \) is applied to each converter with an equal but opposite sign, to adjust the turn-off instant of the corresponding converters. It follows from Fig. 7 that the control circuit with democratic approach is a natural extension of the control circuit with master–slave approach and, therefore, all the implementations presented in Figs. 5, 6, and 14 are applicable with minor modifications.

III. ANALYSIS OF PLL STABILITY

The stability of PLLs can be analyzed by deriving a small-signal model based on the perturbed waveforms such as those in Fig. 3 and by verifying through simulation. To illustrate this method, the master–slave type PLL with cycle-by-cycle instant averaging filter was selected, where the turn-off instant of the slave converter is adjusted by modifying the level of the slave’s feedback error voltage, and where the converters operate with voltage-mode control. The stability of more complex PLLs was analyzed only through simulation.

Considering the perturbed waveforms in Fig. 3 and referring to (4), the following relationships can be obtained:

\[
\Delta T_{\text{sw1}} = \left(1 + \frac{S_{\text{ON}}}{S_{\text{off}}}\right) \cdot \Delta T_{\text{ON1}} = \frac{1}{1 - \left(v_{\text{IN}}/v_{\text{O}}\right)} \cdot \Delta T_{\text{ON1}} \quad (6)
\]

\[
\Delta T_{\text{sw1}} \rightarrow v_{\Delta \text{error1}} \rightarrow \Delta v_{\text{FBerrorS1}} \rightarrow \Delta T_{\text{ON2}} \quad (7)
\]

\[
\Delta T_{\text{sw2}} = \Delta T_{\text{sw1}} + \frac{1}{1 - \left(v_{\text{IN}}/v_{\text{O}}\right)} \Delta T_{\text{ON2}}. \quad (8)
\]

It should be noted in Fig. 3 that \( \Delta T_{\text{ON2}} < 0 \) and, therefore, \( \Delta T_{\text{sw2}} < \Delta T_{\text{sw1}} \). For the 4th perturbed switching cycle

\[
\Delta T_{\text{sw}(k)} = \Delta T_{\text{sw}(k-1)} + \frac{1}{1 - \left(v_{\text{IN}}/v_{\text{O}}\right)} \Delta T_{\text{ON}(k)} \quad (9)
\]

\[
\Delta T_{\text{sw}(k)} \rightarrow v_{\Delta \text{error}(k)} \rightarrow \Delta v_{\text{FBerrorS}(k)} \rightarrow \Delta T_{\text{ON}(k+1)}. \quad (10)
\]

Based on (6)–(10), the corresponding PLL can be represented in the \( s \)-domain, as shown in Fig. 8, where \( S_{\Delta \text{error}} \) is the slope of the voltage ramp for converting \( \Delta T_{\text{sw}} \) to phase-error voltage \( v_{\Delta \text{error}} \), \( S_{\text{PWM}} \) is the slope of the PWM voltage ramp, and \( G_{\text{adj}} \) is the gain of the slave’s turn-off adjustment circuit defined by (4). The delay block \( e^{-sT_{\text{sw}}} \) represents the delay of the \( \Delta T_{\text{sw}} \) perturbation with respect to the \( \Delta T_{\text{ON}} \) perturbation [25], whereas, \( H_{\text{SH}}(s) \) is the sample and hold block

\[
H_{\text{SH}}(s) = \frac{1}{sT_{\text{sw}}} e^{-sT_{\text{sw}}} \quad (11)
\]

If the PLL is much faster than the voltage loop, feedback error voltage \( v_{\text{FBerror}} \) in Fig. 8 can be considered as constant and the loop gain is obtained as

\[
LG_{\text{PLL}}(s) = K_{\text{PLL}} \frac{1 - e^{-sT_{\text{sw}}}}{1 - e^{-sT_{\text{sw}}}} = \frac{K_{\text{PLL}}}{T_{\text{sw}}} e^{-sT_{\text{sw}}} \quad (12)
\]

where

\[
K_{\text{PLL}} = \frac{1}{G_{\text{adj}}} \frac{S_{\Delta \text{error}}}{S_{\text{PWM}}} \quad (13)
\]

The switching period \( T_{\text{sw}} \) in (12) is determined as [4], [5]

\[
T_{\text{sw}} = \frac{L_{B}}{\eta V_{\text{in}}^{2}} P_{\text{in}} \frac{1}{1 - \left(v_{\text{IN}}/v_{\text{O}}\right)} \quad (14)
\]

where \( \eta = P_{\text{O}}/P_{\text{in}} \). It follows from (12) to (14) that the PLL gain is independent of the instantaneous line voltage \( v_{\text{IN}} \).

It can be concluded from (12) that the PLL basically behaves as an integrator. The magnitude and phase of the loop gain (12) are shown in Fig. 9 (line with “o” symbol).

To verify the small-signal model in Fig. 8, SIMPLIS simulations were performed of a 400-V/280-W, 127-Vdc input, interleaved DCM/CCM boundary boost converter with a PLL-based control.
voltage-mode control, where the slave’s turn-OFF instant is adjusted by modifying the slave’s feedback error voltage. The schematic of the simulation circuit is shown in Fig. 10, where the power stage and voltage loop error amplifier are not shown for simplicity. Fig. 10 includes both an implementation of a cycle-by-cycle instant averaging filter, and an implementation of an RC filter, as well as a means of implementing either the master–slave or democratic interleaving method. The PLL gain was simulated by inserting ac voltage source $v_{inj}$.

The instant averaging filter was implemented by using a sawtooth oscillator and two sample and hold (S&H) circuits. The sawtooth oscillator consists of a 100-µA current source and a 1-nF capacitor ($C_{OSC}$) that results in a constant slope, with synchronization to converter 2 through a MOSFET that discharges capacitor $C_{OSC}$ at the rising edge of its gate-drive signal after a short delay. Prior to discharging capacitor $C_{OSC}$, the peak of the sawtooth oscillator is sampled by S&H 1, which is triggered by the rising edge of the output of SR flip-flop FF, and the value is divided by two. When converter 1 turns on, output $Q$ goes low, and a sample of the sawtooth ramp is taken. Phase-error voltage $v_{\Delta \text{err}_{\text{ror}}}$ is obtained by subtracting the output of S&H 2 from half of the output of S&H 1, and therefore, it is proportional to the cycle-by-cycle instant average of output $Q$ minus $V_{CC}/2$, and remains constant over half a switching cycle. Alternatively, the average can also be obtained using an RC filter, and voltage $v_{\Delta \text{err}_{\text{ror}}}$ can be obtained by subtracting $V_{CC}/2$. It should be noted that a gain of 1/24 is included in the RC filter implementation in order to match the dc gain of the instant averaging filter. Voltage $\Delta v_{\text{FBerror1}}$ is obtained through gain $G_{adj1}$, which is set to −0.086 for the master–slave and −0.043 for the democratic control method. Similarly, voltage $\Delta v_{\text{FBerror2}}$ is obtained through gain $G_{adj2}$, which is set to zero for the master–slave, and 0.043 for the democratic control method. Finally, voltages $\Delta v_{\text{FBerror1,2}}$ are summed with the output of the voltage error amplifier ($v_{\text{FBerror}}$), and compared to a PWM ramp with a 0.2-V/µs slope in order to determine the ON-time of each converter.

Simulation results for the master–slave interleaving method are shown in Fig. 9. For the implementation with the cycle-by-cycle instant averaging filter, the simulation results are in excellent agreement with the analytical results, as shown in Fig. 9, which verifies the proposed model. Fig. 9 also includes simulations of the PLL gain using an RC filter with two reasonable filter bandwidths. It is shown that the loop gain with the RC filter, in addition to the integrator, also contains a pole at the RC-filter bandwidth as well as a limited low frequency gain. It should be noted that the positive phase shift at high frequencies in Fig. 9 is caused by the sample-and-hold effect. Since for the implementation with the cycle-by-cycle instant averaging filter only one pole exists and for the implementation with the RC filter only two poles are apparent, it can be concluded that the PLL-based master–slave interleaving methods are always stable. Although the results in Fig. 9 were obtained for voltage-mode control where the turn-OFF instant of the slave is adjusted by modifying the slave’s feedback error voltage, similar results can be obtained for current-mode control as well as for both voltage-mode and current-mode control methods with the adjustment of the slope of the slave’s PWM ramp.

Simulation results comparing the stability of PLLs of master–slave and democratic interleaving methods are shown in Fig. 11. It is shown in Fig. 11 that the PLL gain of the democratic interleaving method is nearly identical to that of the master–slave interleaving method except for a minor phase mismatch at high frequencies for the implementation with instant averaging.
filter. In fact, the democratic interleaving method with instant averaging filter has slightly larger phase shift at high frequencies than the master–slave interleaving method, which is the result of the slightly changing switching frequency in two consecutive switching cycles after a perturbation. In that case, the terms $1 - e^{-sT_{sw}}$ in the numerator and denominator of (12) are not completely cancelled.

IV. DYNAMIC RESPONSE OF PLL

To compare the dynamic response of the implementations with instant averaging filter and $RC$ filter, time-domain simulations were performed using the simulation circuit in Fig. 10. The results are presented in Fig. 12. A perturbation was injected using an 80-mV voltage pulse through voltage source $v_{pert}$ in Fig. 10 to increase the feedback error voltage during a single switching cycle. It can be seen in Fig. 12 that the implementation with the instant averaging filter recovers from the perturbation at least twice as fast as the implementation with the $RC$ filter. It should be noted in Fig. 12 that the shape of the perturbed phase-error voltage is consistent with the order of the corresponding implementation. Fig. 12 also illustrates that the dynamic response of the master–slave and democratic interleaving methods is nearly identical.

Simulation results presented in Fig. 13 illustrate that the dynamic response of the master–slave and democratic interleaving methods remains nearly identical when an ac input voltage is applied. The SIMPLIS simulation circuit, shown in Fig. 14, modeled a 385-V/250-W, universal input, interleaved DCM/CCM boundary boost PFC converter that operates with a PLL-based current-mode control circuit, where the turn-OFF instant is adjusted by modifying the slope of the current sense voltage ramp, and where the converters operate with current-mode control ($V_{IN} = 90 \, V_{rms}$).

The simulation circuit in Fig. 14 is based on the L6563 controller from ST Microelectronics, which operates with a master–slave relationship when mode selection voltage $V_{MODE} = 1$, and which operates with a democratic relationship when $V_{MODE} = 0$. It should be noted that transconductance gain $K$ is set to 1 when operated with a master–slave relationship, and 0.5 when operated with a democratic relationship. The slope adjustment is accomplished by making the added voltage ramp proportional to rectified input voltage $v_{rec}$ so that adjusted current sense ramp $v_{CSadj}$ is proportional to rectified input voltage $v_{rec}$.

The dynamic response was tested by perturbing the reference current of converter 1, i.e., by increasing the level of feedback voltage of converter 1 by 100 mV for a single switching cycle at the peak of the input voltage, at full load, and $V_{IN} = 90 \, V_{rms}$. The perturbation in Fig. 13 damps with a settling time approximately equal to 1.5 ms. It should be noted that this control method, namely synchronization to the turn-OFF instant with
which can be considered as a natural perturbation [21], and that interleaving is lost around the zero crossing of the line voltage, with turn-OFF synchronization. It is shown in Fig. 15 that in-terleaves with voltage-mode control using a democratic approach.

In the range, interleaved prototype converter implemented with the results were obtained on a 400-V/300-W, universal input inductor current waveforms during a line cycle. The experimen-tability of the interleaved DCM/CCM boundary boost PFC con-}

current-mode control, is unstable when implemented with open-loop control, as shown in [19].

Finally, experimental results shown in Fig. 15 verify the sta-bility of the interleaved DCM/CCM boundary boost PFC con-}

verters with PLL-based closed-loop control by observing the inductor current waveforms during a line cycle. The experimen-tal results were obtained on a 400-V/300-W, universal input range, interleaved prototype converter implemented with the UCC28061 interleaving IC controller [24]. The prototype operates with voltage-mode control using a democratic approach with turn-OFF synchronization. It is shown in Fig. 15 that inter-leaving is lost around the zero crossing of the line voltage, which can be considered as a natural perturbation [21], and that interleaving is restored around the peak of the line voltage.

V. SUMMARY

A systematic review of PLL-based closed-loop control meth-ods for interleaved DCM/CCM boundary boost PFC converters has been presented. A small-signal model of the PLL with an instant averaging filter was developed and verified by simula-tion. The stability of the PLL with instant averaging filter and RC filter was demonstrated by simulation in both frequency and time domain. Based on the simulation results, it was con-cluded that the PLL-based closed-loop methods always provide stable operation. It was also shown that the dynamic response of the PLL-based closed-loop methods with master–slave approach and democratic approach is almost identical. Experimen-tal results obtained on a 300-W, universal input, interleaved DCM/CCM boundary boost PFC prototype circuit with a dedicated controller IC utilizing a democratic, PLL-based closed-loop method were also provided.

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Fig. 15. Measurements of a 400-V/300-W, universal input, interleaved DCM/CCM boundary boost PFC converter with PLL-based closed-loop control circuit using democratic interleaving method, where the converters operate with voltage-mode control.


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