

Fully Soft-Switched Three-Stage AC–DC Converter

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Abstract—The paper presents a fully soft-switched three-stage ac–dc power supply for server applications. In this three-stage architecture, the front-end boost power factor correction (PFC) is followed by a dc–dc boost converter that serves as a preregulator to the isolated dc–dc output stage. Through magnetic integration, soft switching of all semiconductor switches in the PFC boost converter and the dc–dc boost preregulator is achieved in addition to a reduced number of magnetic components. Generally, the output dc–dc stage can be implemented with any isolated topology. In this development, a zero voltage switching half-bridge dc–dc converter is employed for the third stage. The performance of the proposed three-stage approach was evaluated on a 700-W/12-V, universal-line-range ac–dc prototype.

Index Terms—Boost converter, holdup time, power factor correction (PFC), soft switching, three stages.

I. INTRODUCTION

A FRONT-END power-factor-corrected (PFC) boost converter followed by a dc–dc output stage is the architecture that has been almost exclusively used in offline power supplies for computer and telecom applications. The front-end boost rectifier is employed to reduce the line-current harmonics and provide compliance with various worldwide specifications governing the harmonic limits of the line current in offline power supplies, whereas the dc–dc output power stage is employed to provide galvanic isolation and tight output voltage regulation.

Although for many years the performance of this two-stage architecture, shown in Fig. 1(a), has been continuously improved to meet the challenges of ever-increasing power density and efficiency requirements, its potential to meet future power density and efficiency requirements of power supplies that must also meet a holdup time requirement may be limited. The major performance limitation of the two-stage architecture stems from a suboptimal design of the dc–dc isolation stage. Namely, for power supplies with holdup time requirement, the dc–dc output stage must be designed with an input-voltage range that is wide enough to regulate output voltage during a line dropout by discharging the energy-storage (bulk) capacitor. Since there is a strong tradeoff between the size of the bulk capacitor and the input-voltage range of the dc–dc output stage, the input-voltage range of the dc–dc output stage in high-density power supplies is relatively large, i.e., it is typically from 300 to 400 V. Because the dc–dc output stage needs to be designed for a relatively wide input-voltage range, its performance is not optimal. Specifically, the increased input-voltage range requires that the turns ratio

of the transformer is reduced, which increases the conduction losses on the primary side and increases voltage stresses on the semiconductor components on the secondary side. Moreover, the increased secondary-side voltage stresses usually mandate the use of components with higher voltage ratings that are typically less efficient.

To obtain the optimal performance of the isolated dc–dc stage, its input voltage should be constant. This ideal input-voltage requirement can be achieved by resorting to the three-stage architecture shown in Fig. 1(b). In this three-stage architecture, the front-end PFC stage is followed by a dc–dc stage that serves as a preregulator to the dc–dc isolated output stage. Because of the preregulator, the input voltage to the output stage is always kept constant, even during the holdup time.

Although the three-stage architecture resolves the tradeoff between the bulk capacitor size and the performance of the isolated dc–dc stage in an optimal way, it is still not clear if and in what applications the overall power density and efficiency performance of the three-stage approach is better than that of the two-stage approach. The main reason for this ambiguity is the fact that the dc–dc preregulation stage introduces losses and requires space for implementation. According to results presented in [1], for applications where the dc input voltage variations are more than 10%, the combined efficiency of a dc–dc preregulator and the isolated dc–dc output stage can be higher than that of the isolated dc–dc output stage alone. In fact, commercially available high-power-density, high-efficiency, multistage, dc–dc converters that utilize a dc–dc bulk preregulator and two interleaved forward converters exist today [2]. Nevertheless, more comprehensive and thorough research and evaluation are needed to understand the performance of ac–dc power supplies implemented with a three-stage approach compared to those implemented with the conventional two-stage approach.

It should also be noted that besides the described three-stage ac–dc power supply architecture where the second stage employs a nonisolated topology and the third stage an isolated topology, the three-stage architecture can be implemented with an isolated second stage and a nonisolated third stage. In this implementation, the second-stage isolated converter operates as a dc–dc transformer and the nonisolated third stage provides regulation.

Generally, any nonisolated or isolated topology can be used to implement corresponding stages. However, to reduce switching losses and improve electromagnetic compatibility performance, it is desirable to employ soft-switching topologies. While many soft-switching, isolated dc–dc topologies are available [3]–[10], nonisolated soft-switching topologies that do not suffer from undue complexity are still not available. As a result, nonisolated dc–dc stages in [1] and [2] are implemented with conventional “hard”-switched topologies.

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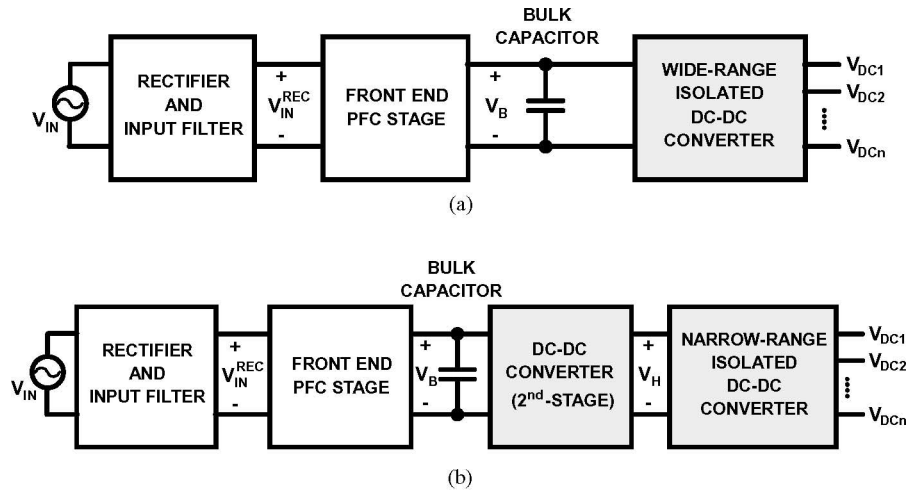


Fig. 1. Block diagram of a typical ac–dc power supply.

This paper presents a fully soft-switched three-stage ac–dc power supply that employs a dc–dc boost converter as the second-stage preregulator. Soft switching of this second-stage boost converter is achieved by its integration with a soft-switched boost PFC rectifier described in [11] through magnetic integration similar to that described in [12] for the flyback converter integration. The proposed magnetically integrated PFC boost and dc–dc boost converters feature soft switching of all semiconductors. The boost switches in both converters are turned on while the switch body diode is conducting, i.e., zero voltage switching (ZVS), whereas the active snubber switch of the PFC boost converter turns off after its drain current has reached zero, i.e., zero current switching (ZCS). In addition, the boost rectifiers in both converters are turned off softly with a controlled di/dt rate so that reverse-recovery-related losses of the boost rectifiers are virtually eliminated, enabling the use of slower and cheaper fast-recovery rectifiers. In this development, the dc–dc isolated output stage was implemented with a ZVS half-bridge dc–dc converter.

II. SOFT-SWITCHED PFC BOOST CONVERTER WITH AN INTEGRATED SECOND-STAGE BOOST CONVERTER

The proposed soft-switched boost converter magnetically integrated with a dc–dc boost converter is shown in Fig. 2. The boost converter consists of voltage source V_{IN}^{REC} , boost inductor L_B , main switch S , boost rectifier D , energy-storage capacitor C_B , the active snubber circuit formed by auxiliary switch S_1 , winding N_1 of coupled inductor L_D , snubber inductor L_S , and blocking diode D_1 . The second-stage boost converter consists of switch S_D with an associated antiparallel diode, winding N_2 of coupled inductor L_D , output rectifier D_D , and output capacitor C_F .

To facilitate the explanation of the circuit operation, Fig. 3 shows a simplified circuit diagram of the proposed converter in Fig. 2. In the simplified circuit, energy-storage capacitor C_B and output filter capacitor C_F are modeled by voltage sources V_B and V_O by assuming that the values of C_B and C_F are large enough so that the voltage ripples across the capacitors

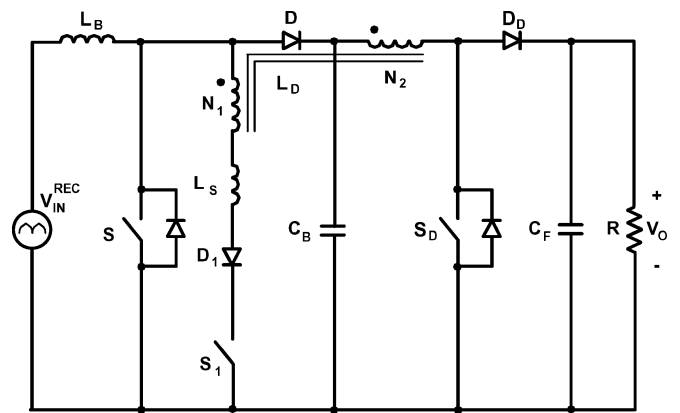


Fig. 2. Soft-switched power supply that integrates a PFC boost converter and a dc–dc boost converter.

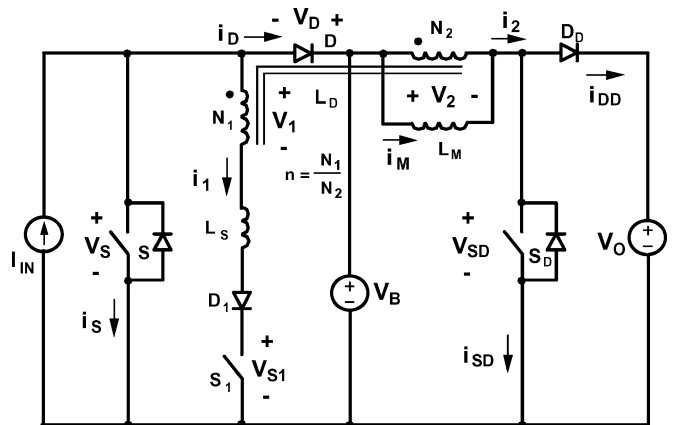


Fig. 3. Simplified circuit diagram along with reference directions of key currents and voltages.

are small in comparison to their dc voltages. In addition, boost inductor L_B is modeled as constant current source I_{IN} by assuming that the inductance of L_B is large so that during a switching cycle, the current through L_B does not change significantly. In this analysis, the leakage inductance of the coupled

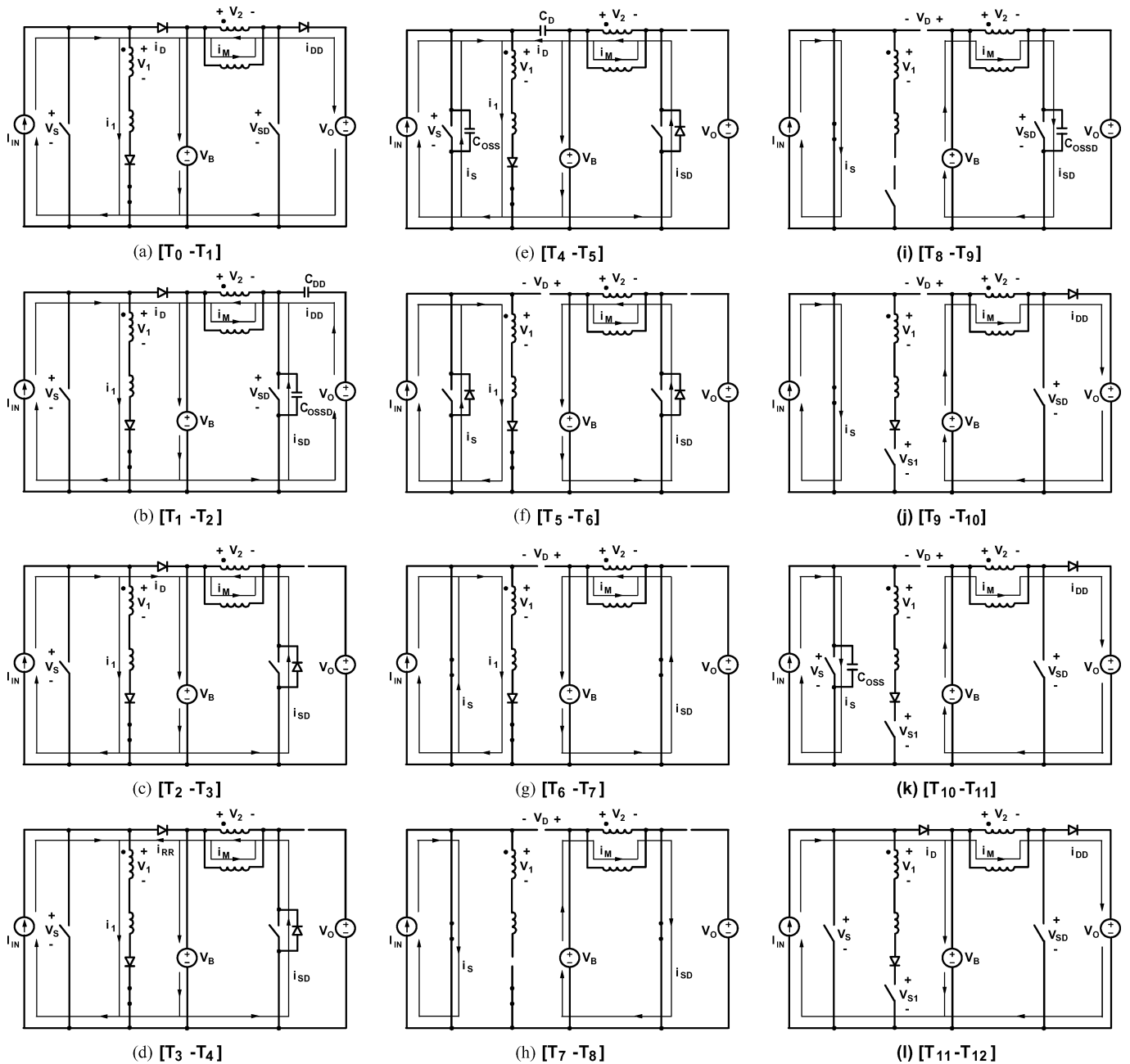


Fig. 4. Topological stages during a switching period.

inductor is neglected since it does not have a significant effect on the operation of the circuit. Moreover, since snubber inductor L_S and primary winding N_1 of coupled inductor L_D are connected in series, the leakage inductance of the coupled inductor is absorbed by L_S . As a result, coupled inductor L_D is modeled by magnetizing inductance L_M and the two-winding ideal transformer. Finally, it is assumed that in the ON state, the semiconductors exhibit zero resistance, i.e., they are short circuits. However, the output capacitance of the switches, as well as the junction capacitance and the reverse-recovery charge of the boost rectifier are not neglected in this analysis.

To further facilitate the analysis of operation, Fig. 4 shows the major topological stages of the circuit in Fig. 2 during a switching cycle, whereas Fig. 5 shows its key waveforms. The

reference directions of currents and voltages plotted in Fig. 5 are shown in Fig. 3.

As can be seen from the timing diagrams in Fig. 5(a)–(c), the turn-on of PFC boost switch S and of second-stage boost switch S_D are synchronized, whereas auxiliary switch S_1 is turned on prior to the turn-on of switches S and S_D . In addition, auxiliary switch S_1 is turned off before PFC boost switch S or second-stage boost switch S_D is turned off, i.e., the proposed circuit operates with overlapping gate drive signals for the active snubber switch and the converter switches.

Prior to the turn-on of switch S_1 at $t = T_0$, all switches are open. As a result, the entire input current I_{IN} flows through boost rectifier D into energy-storage capacitor C_B in the boost power stage, while magnetizing current i_M flows through

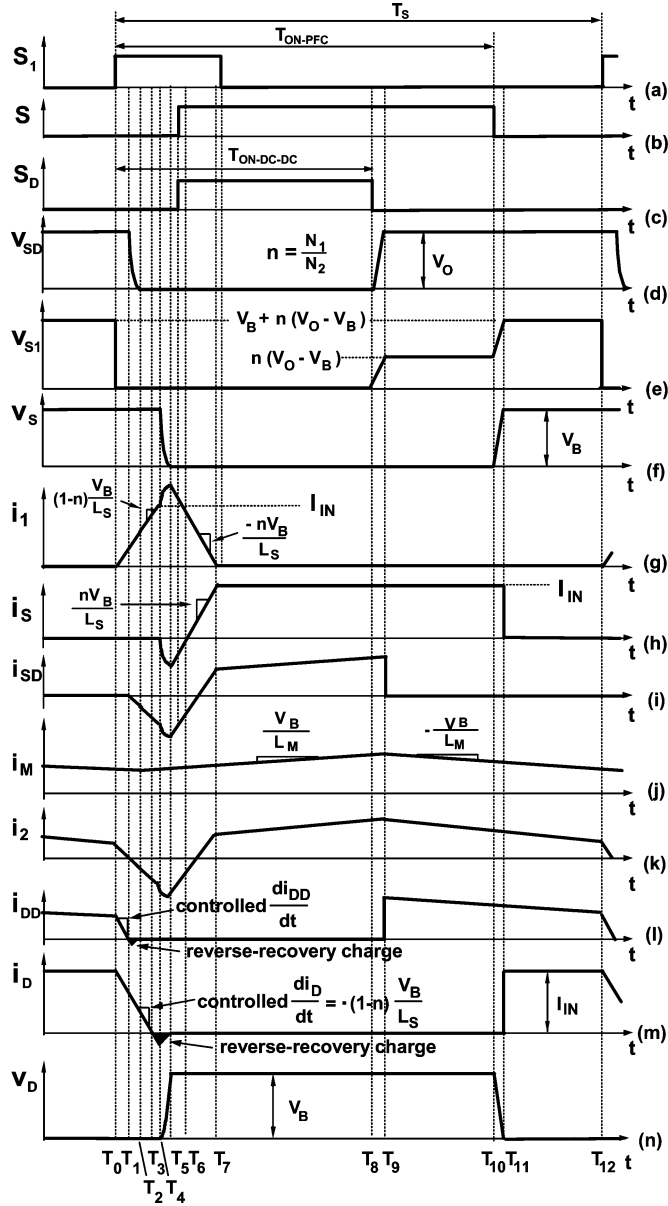


Fig. 5. Key waveforms.

output rectifier D_D in the second-stage boost converter, as shown in Fig. 4(l). Because output rectifier D_D is conducting during this period, the induced voltage across winding N_1 of coupled inductor L_D is $n(V_B - V_O)$, i.e., $v_1 = nv_2 = n(V_B - V_O)$, where $n = N_1/N_2$. After switch S_1 is turned on at $t = T_0$, the voltage of energy-storage capacitor V_B and induced voltage $n(V_B - V_O)$ are applied across snubber inductor L_S so that current i_1 starts to increase linearly, as illustrated in Fig. 5(g). The slope of current i_1 is

$$\frac{di_1}{dt} = \frac{V_B - v_1}{L_S} = \frac{V_B + n(V_O - V_B)}{L_S}. \quad (1)$$

As current i_1 starts flowing through winding N_1 of coupled inductor L_D , magnetizing current i_M begins to divert from output rectifier D_D to winding N_2 , i.e., $i_{DD} = i_M - ni_1$, as shown

in Figs. 4(a) and 5(l). Current i_{DD} decreases until it becomes zero and output rectifier D_D turns off at $t = T_1$.

As current i_1 increases linearly, output rectifier current i_{DD} decreases linearly at the same rate since the sum of ni_1 and i_{DD} is equal to magnetizing current i_M that is relatively constant, i.e., $ni_1 + i_{DD} = i_M$. Therefore, in the proposed circuit, the turn-off rate of the boost rectifier

$$\frac{di_{DD}}{dt} \cong -n \left(\frac{V_B + n(V_O - V_B)}{L_S} \right) \quad (2)$$

can be controlled by the proper selection of the inductance value of snubber inductor L_S and turns ratio n of coupled inductor L_D . Typically, for today's fast-recovery rectifiers, the turn-off rate di_D/dt should be kept around $100 \text{ A}/\mu\text{s}$. With such a selected turn-off rate, the reverse-recovery current of the rectifier and the related power losses and electromagnetic interference (EMI) problems are minimized.

Since output rectifier current i_{DD} is zero after $t = T_1$, the increasing current in winding N_1 makes the current in winding N_2 larger than magnetizing current i_M . This excessive current discharges output capacitance C_{OSSD} of switch S_D and charges output capacitance C_{DD} of rectifier D_D , as illustrated in Figs. 4(b) and 5(d). During this period, voltage v_2 across winding N_2 of coupled inductor L_D starts to increase. After the output capacitance of switch S_D is fully discharged at $t = T_2$, current i_{SD} continues to flow through the antiparallel diode of switch S_D , as shown in Figs. 4(c) and 5(i). To achieve ZVS of S_D , switch S_D should be turned on while its antiparallel diode is conducting. To simplify the control circuit timing diagram, the turn-on of switch S_D is synchronized with the turn-on of boost switch S . When the antiparallel diode of switch S_D is conducting, voltage v_2 across winding N_2 is equal to V_B so that induced voltage v_1 on winding N_1 is

$$v_1 = \frac{N_1}{N_2} V_B = nV_B. \quad (3)$$

Since v_1 is constant, voltage applied across snubber inductor L_S is also constant so that current i_1 increases linearly with a slope of

$$\frac{di_1}{dt} = \frac{V_B - v_1}{L_S} = \frac{V_B - nV_B}{L_S} = (1 - n) \frac{V_B}{L_S}. \quad (4)$$

During the same period, magnetizing inductance i_M increases with a slope given by

$$\frac{di_M}{dt} = \frac{V_B}{L_M}. \quad (5)$$

As current i_1 increases linearly, boost rectifier current i_D decreases linearly at the same rate since the sum of i_1 and i_D is equal to constant input current I_{IN} , i.e., $i_1 + i_D = I_{IN}$. Therefore, in the proposed circuit, the turn-off rate of the boost rectifier

$$\frac{di_D}{dt} = -(1 - n) \frac{V_B}{L_S} \quad (6)$$

can also be controlled by the proper selection of the inductance value of snubber inductor L_S and turns ratio n of coupled inductor L_D .

The topological stage in Fig. 4(c) ends at $t = T_3$ when the current of boost rectifier D becomes zero. During the time period between $t = T_3$ and $t = T_4$, the reverse-recovery current of boost rectifier D flows through snubber inductor L_S . After $t = T_4$, current i_1 starts to discharge the output capacitance of boost switch S and charge junction capacitance C_D of boost rectifier D , as shown in Fig. 4(e). If the turns ratio of coupled inductor L_D is selected so that $n < 0.5$, the energy stored in L_S is sufficient to completely discharge the output capacitance of boost switch S regardless of the load and line conditions. Once the capacitance is fully discharged at $t = T_5$, current i_S continues to flow through the antiparallel diode of boost switch S , as shown in Figs. 4(f) and 5(h). During this period, voltage v_1 is applied in the negative direction across snubber inductor L_S . Therefore, current i_1 starts to decrease linearly at the rate given by

$$\frac{di_1}{dt} = -\frac{nV_B}{L_S} \quad (7)$$

as illustrated in Fig. 5(g). The current in auxiliary switch S_1 also starts to decrease, whereas boost switch current i_S starts to increase from the negative peak value, as shown in Fig. 5(g) and (h). To achieve ZVS of boost switch S , it is necessary to turn on boost switch S before its current becomes positive at $t = T_6$, i.e., during the period when current i_S still flows through the antiparallel diode of switch S , as illustrated in Fig. 5(h).

As shown in Fig. 5(g), current i_1 continues to decrease until it reaches zero at $t = T_7$. Shortly after $t = T_7$, auxiliary switch S_1 is turned off to achieve ZCS. After switch S_1 is turned off, the entire input current I_{IN} flows through boost switch S . As a result, the front-end boost converter stage is completely decoupled from the second-stage boost converter, as shown in Fig. 4(h). For the rest of the switching cycle, the PFC boost and second-stage boost converters continue to operate as conventional boost converters.

After second-stage boost switch S_D is turned off at $t = T_8$, magnetizing current i_M starts to charge the output capacitance of switch S_D , as shown in Fig. 4(i). When voltage v_{SD} reaches V_O at $t = T_9$, diode D_D starts to conduct, which forces the commutation of the magnetizing current from switch S_D to output diode D_D , as shown in Fig. 4(j). At the same time, the reset of coupled inductor L_D is initiated by applied voltage $v_2 = V_B - V_O$ across winding N_2 . During the reset time of coupled inductor L_D , voltage v_{SD} across the second-stage boost switch is equal to V_O , whereas the voltage across auxiliary switch S_1 is $v_{S1} = n(V_O - V_B)$ due to the magnetic coupling of windings N_1 and N_2 , as illustrated in Fig. 5(d) and (e).

After boost switch S is turned off at $t = T_{10}$, voltage across switch S starts increasing linearly because constant input current I_{IN} starts charging the output capacitance of boost switch S , as shown in Fig. 4(k). The increasing boost switch voltage causes an equal increase of voltage v_{S1} across auxiliary switch S_1 . When boost switch voltage v_S reaches V_B at $t = T_{11}$, boost diode D begins to conduct, as shown in Fig. 4(l). At the same time, auxiliary switch voltage v_{S1} reaches its maximum value of $v_{S1} = V_B + n(V_O - V_B)$. A small clamping diode can be connected from the drain of auxiliary switch S_1 to output

voltage V_O to eliminate any undesired ringing. The circuit stays in the topological stage shown in Fig. 4(l) until the next switching cycle is initiated at $t = T_{12}$.

In summary, the major feature of the proposed circuit in Fig. 2 is the soft switching of all semiconductor devices. Specifically, PFC boost switch S and second-stage boost switch S_D are turned on with ZVS, whereas auxiliary switch S_1 is turned off with ZCS. In addition, PFC boost diode D and second-stage boost diode D_D are turned off with controlled turn-off rates of their currents. Because all semiconductor components of the proposed converter operate with soft switching, the overall switching losses are minimized, which maximizes the conversion efficiency. In addition, soft switching has a beneficial effect on EMI, and may result in a smaller size input filter.

However, it should be noted that complete ZVS of second-stage boost switch S_D can be achieved only if input current I_{IN} (which is being commutated to winding N_1 when auxiliary switch S_1 is closed) is large enough to produce a negative current through primary winding N_2 and discharge the output capacitance of switch S_D , as shown in Fig. 4(b). According to Fig. 4(b), to have a negative current flowing through winding N_2 after $t = T_1$, reflected current i_1 into winding N_2 has to be greater than magnetizing current i_M . If this condition is not met, switch S_D operates with partial ZVS. This mode of operation typically occurs near the zero crossing of the line voltage in a PFC boost converter. Since the input current is proportional to the line voltage, input current I_{IN} is small near the zero crossing of the line voltage. However, by adding an extra capacitor across boost switch S , switch S_D can achieve complete ZVS near the zero crossing of the line voltage.

Due to the ZVS of the PFC boost switch and the second-stage boost switch, the most suitable implementation of the circuit in Fig. 2 is with the PFC boost switch and the second-stage boost switch consisting of MOSFET devices. Similarly, due to the ZCS of auxiliary switch S_1 , an insulated gate bipolar transistor (IGBT) is suitable for the auxiliary switch.

In the proposed circuit, the voltage stresses on PFC boost switch S and boost rectifier D are identical to the corresponding stresses in the conventional PFC boost converter without a snubber. However, the voltage stress of the second-stage switch S_D and output diode D_D are equal to output voltage V_O that is approximately 10% higher than energy-storage capacitor voltage V_B . The peak voltage of auxiliary switch S_1 is

$$v_{S1(\text{MAX})} = V_B + n(V_O - V_B) < V_O \quad (8)$$

because n is less than 0.5.

The control of the proposed circuit can be performed by two independent controllers that are synchronized. Specifically, one controller is used to regulate the output voltage of the front-end boost stage, i.e., voltage V_B across the energy-storage capacitor C_B . The other controller is used to regulate output voltage V_O of the second-stage boost converter. Any control strategy can be used to control these two voltages, including multiloop control strategies such as various current-mode control implementations. Recently, Texas Instruments (TI) has developed two combo controllers (UCC28521 and UCC28528) for this application.

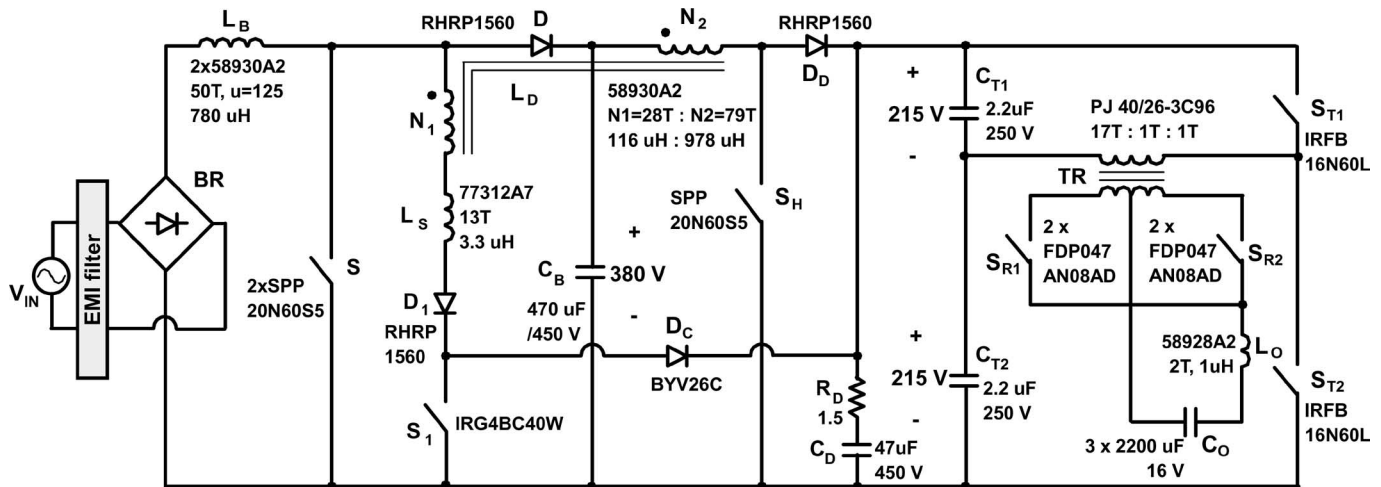


Fig. 6. Schematic diagram of the experimental prototype circuit.

III. EXPERIMENTAL RESULTS

The performance of the proposed soft-switched converter was evaluated on a 700-W three-stage prototype circuit that was designed to operate from a universal ac-line input (90–264 V_{rms}) and deliver up to 58.3 A at a 12-V output. The front-end PFC boost converter with the integrated second-stage boost converter was designed to deliver 430-V, 750-W power to the input of the third-stage dc–dc isolated converter, as shown in Fig. 6. The first-stage and second-stage converters operate at 80 kHz switching frequency. As shown in Fig. 6, a conventional half-bridge converter with synchronous rectifiers is implemented as the third-stage converter that operates at 125 kHz switching frequency. It should be noted that any isolated dc–dc converter topology can be used for the third stage. Moreover, the third-stage converter can be well optimized because it has a very narrow input range.

Fig. 6 shows the schematic diagram and component information of the experimental prototype circuit. Since the drain voltage of boost switch S is clamped to bulk capacitor C_B , the peak voltage stress on boost switch S is approximately 380 V. The peak current stress on switch S , which occurs at full load and low line, is approximately 13.3 A. Therefore, two SPP20N60S5 MOSFETS ($V_{DSS} = 600$ V, $I_{D25} = 20$ A, $R_{DS} = 0.19 \Omega$) from Infineon were used for the boost switch. The maximum drain voltage of second-stage boost switch S_D is $V_{SD(MAX)} = V_O = 430$ V, as shown in Fig. 5(d). Since the peak current stress on second-stage boost switch S_D is approximately 2.1 A, an SPP20N60S5 MOSFET was used for S_D . Finally, a high-speed IRG4BC40W IGBT ($V_{RRM} = 600$ V, $I_F = 40$ A) from IR was used as auxiliary switch S_1 since its maximum drain voltage is $V_{S1(MAX)} = V_B + n(V_O - V_B) = 380 + 0.35 \times (430 - 380) = 398$ V, as shown in (8). Moreover, diode D_C clamps auxiliary switch S_1 to capacitors C_{T1} and C_{T2} , as shown in Fig. 6.

Since boost diodes D must block the bulk voltage and must conduct the peak input current, which is approximately 13.3 A, an RHRP1560 diode ($V_{RRM} = 600$ V, $I_{FAVM} = 15$ A) from Fairchild was used as boost diode D . An RHRP1560 diode was used for diode D_1 and another RHRP1560 for D_D .

To obtain the desired inductance of boost inductor L_B of approximately 780 μ H, the boost inductor was built using two parallel toroidal high-flux cores (58930A2) from Magnetics and 50 turns of magnet wire (AWG #16).

External snubber inductor L_S was connected in series with winding N_1 of coupled inductor L_D , as shown in Fig. 6. The required inductance is approximately 3.3 μ H. Snubber inductor L_S was built using a toroidal Kool- μ core (77312A7) from Magnetics and 13 turns of magnet wire (AWG #16).

Coupled inductor L_D was built using a toroidal high-flux core (58930A2), 28 turns of magnet wire (AWG #17) for winding N_1 , and 79 turns of magnet wire (AWG #19) for winding N_2 . Magnetizing inductance L_M measured across winding N_2 of coupled inductor L_D is approximately 978 μ H.

A high-voltage aluminum capacitor (470 μ F, 450 V_{dc}) was used for bulk capacitor C_B to meet the holdup time requirement. Two film capacitors (2.2 μ F, 250 V_{dc}) are used for half-bridge capacitors C_{T1} and C_{T2} , respectively. A small R – C damping circuit that consists of capacitor C_D and resistor R_D is connected across capacitors C_{T1} and C_{T2} to eliminate input oscillations of the third-stage converter.

The third-stage half-bridge converter was implemented with an IRFB16N60 L MOSFET from IR for each of bridge switches S_{T1} and S_{T2} , two parallel FDP047AN08AD MOSFETS from Fairchild for each of synchronous rectifier switches S_{R1} and S_{R2} . Transformer TR was built using a pair of ferrite cores (PJ 40/26-3C96) with 17 turns of magnet wire (AWG #16) for the primary winding and 1 turn of copper foil (10 ml, 15 mm) for each of the secondary windings. Output filter inductor L_O was built using a toroidal high-flux core (58928A2) from Magnetics and two turns of magnet wire (4 \times AWG #17). Three low-voltage aluminum capacitors (2200 μ F, 16V_{dc}) were used for output capacitor C_F .

The performance of the proposed soft-switched converter was verified by comparing the efficiencies of the prototype circuit with and without the active snubber circuit. To measure the efficiency of the experimental converter without the active snubber circuit, switch S_1 , diode D_1 , inductor L_S , and winding N_1 of the prototype circuit shown in Fig. 6 are disconnected. Moreover,

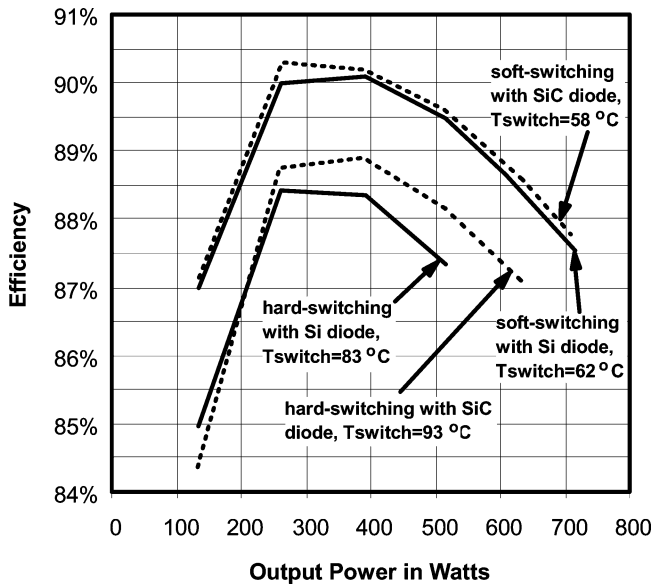


Fig. 7. Measured efficiencies of the experimental three-stage converter delivering 12-V output from 90- V_{ac} input.

the efficiencies of the prototype circuit using recently developed CSD10060 silicon-carbide (SiC) diodes from CREE for PFC boost diode D and second-stage boost diode D_D are also measured. Fig. 7 shows the measured efficiencies of the experimental converter with and without the active snubber circuit as functions of the output power of PFC front end. The figure also shows the measured efficiencies with silicon diodes or SiC diodes. As can be seen in Fig. 7, the active snubber improves the conversion efficiency in the entire measured power range. The efficiency improvement is more pronounced at higher power levels where the reverse-recovery losses are greater. The prototype circuit without an active snubber cannot deliver more than 550 W because the junction temperature of the PFC boost switch exceeds its limit. By using SiC diodes for D and D_D , the prototype circuit without active snubber can deliver up to 650 W, which is still lower than full power. It should be noted that the efficiencies of the prototype circuit using silicon diodes or SiC diodes are not much different as long as the proposed active snubber circuit is incorporated.

Fig. 7 also shows the important advantage of the integrated magnetic approach utilized in the proposed converter. By using coupled inductor L_D as shown in Fig. 6, magnetic energy can be stored in coupled inductor L_D by both switches S_1 and S_D . During the period when auxiliary switch S_1 is ON, the coupled inductor provides a direct energy path to the second boost stage that bypasses bulk capacitor C_B and boost diode D of the first boost stage. Since this direct energy coupling path reduces the current in both diode D and switch S_D , the conduction losses in the PFC boost diode D and second-stage boost switch S_D are reduced.

Performance of the two-stage approach is compared to that of the proposed three-stage approach. Fig. 8 shows the measured efficiencies of a hard-switching two-stage approach and the proposed soft-switching three-stage approach. To measure the efficiency of the two-stage approach, the second-stage boost converter and the soft-switching circuit of the experimental cir-

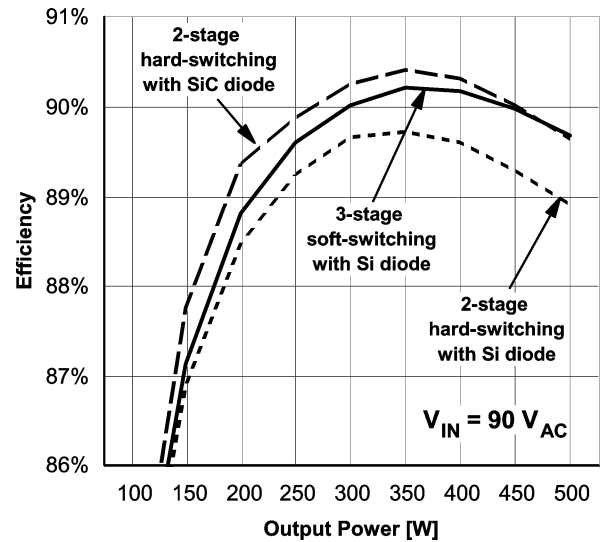


Fig. 8. Measured efficiencies of the experimental two-stage and three-stage converters delivering 12-V output from 90- V_{ac} input.

cuit in Fig. 6 are removed. The proposed three-stage rectifier shows better efficiency than the hard-switching two-stage rectifier if both the approaches utilize silicon diodes. If a SiC diode is utilized as a PFC boost diode in the two-stage approach, its efficiency is better than that of the proposed three-stage approach at light load. It should be noted that the tested two-stage approach does not tightly regulate the output voltage because the second-stage dc-dc transformer in Fig. 6 was not designed to regulate its output. If the dc-dc transformer is redesigned to achieve an output regulation, the efficiency of the two-stage approach is expected to be lower than the results shown in Fig. 8. To regulate the output, the turns ratio of transformer TR should be reduced, which results in greater conduction and switching losses at the primary of transformer TR.

Figs. 9 and 10 show the oscillograms of key waveforms in the experimental converter when it delivers full power from the low line input voltage. As can be seen from the corresponding waveforms in Fig. 5, there is a good agreement between the experimental and theoretical waveforms. As can be seen from Figs. 9 and 10, switches S and S_D are turned on with ZVS since their voltages V_S and V_{SD} fall to zero before gate-drive signals V_{GS} and V_{GSD} become high. Moreover, auxiliary switch S_1 achieves soft-switching turn-off because switch current i_1 becomes zero before auxiliary switch S_1 is turned off. It should also be noted that the slope of rectifier current i_D is approximately $di/dt = 70 \text{ A}/\mu\text{s}$ during the period when boost diode D is turned off. The rectifier-current slope is controlled by snubber inductance L_S , as indicated in Figs. 9 and 10. With this di/dt rate, peak reverse-recovery current I_{RR} is reduced to approximately 1.5 A.

Fig. 11 shows the measured waveforms of bulk capacitor voltage V_B and output voltage V_O of the second-stage boost converter. Because the second-stage boost converter can maintain its output voltage from the peak bulk capacitor voltage $V_{B-PEAK} = 380 \text{ V}$ to near 120 V, approximately 90% of the stored energy in C_B is utilized for a holdup time. The measured holdup time is approximately 30 ms, as shown in Fig. 11.

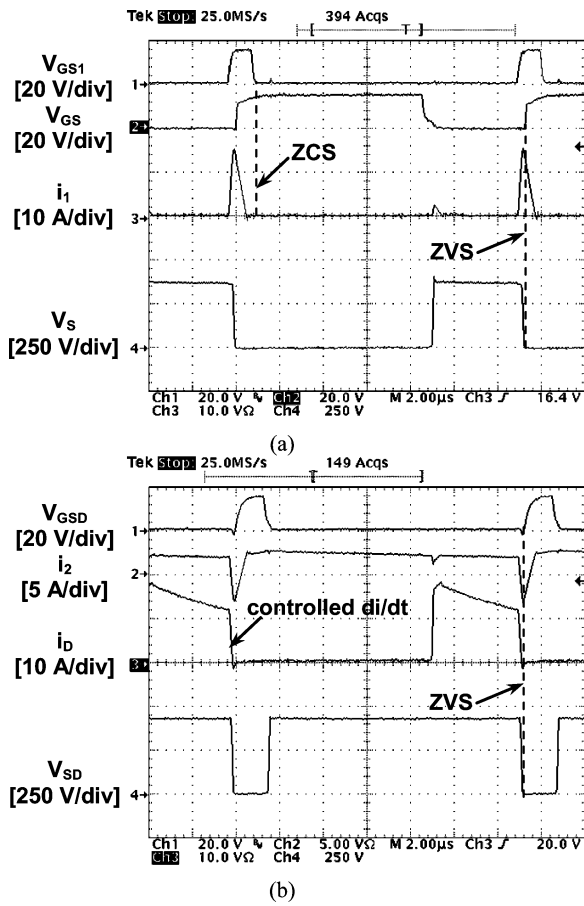


Fig. 9. Measured waveforms of the proposed circuit at $V_{IN} = 90\text{ V}$, $V_B = 380\text{ V}$, $V_O = 430\text{ V}$, $V_{dc} = 12\text{ V}$, $P_{dc} = 700\text{ W}$. Time base: $2\ \mu\text{s}/\text{div}$.

Since all switches operate with ZVS or ZCS switching, the rectifier reduces switching losses and is also expected to improve EMI.

IV. CONCLUSION

A fully soft-switched three-stage ac-dc power supply for server applications has been introduced. In this three-stage architecture, the front-end boost PFC is followed by a dc-dc boost converter that serves as a preregulator to the isolated dc-dc output stage. By using a single magnetic device, which is mutually shared by the PFC boost converter and the dc-dc boost converter, PFC boost switch S and second-stage boost switch S_D are turned on with ZVS, auxiliary switch S_1 is turned off with ZCS, and boost diodes D and D_D are turned off softly using a controlled di/dt rate. As a result, the turn-on switching losses in the boost switches, the turn-off switching loss in the auxiliary switch, and reverse-recovery-related losses in the boost diodes are eliminated, which maximizes the conversion efficiency. A ZVS half-bridge dc-dc converter is employed for the third stage. The performance of the proposed converter was verified on a 700-W/12-V prototype circuit that was designed to operate from a universal ac-line input. The proposed soft-switching technique improves the efficiency by approximately 2% at 700 W in comparison to the efficiency of the conventional hard-switching converter.

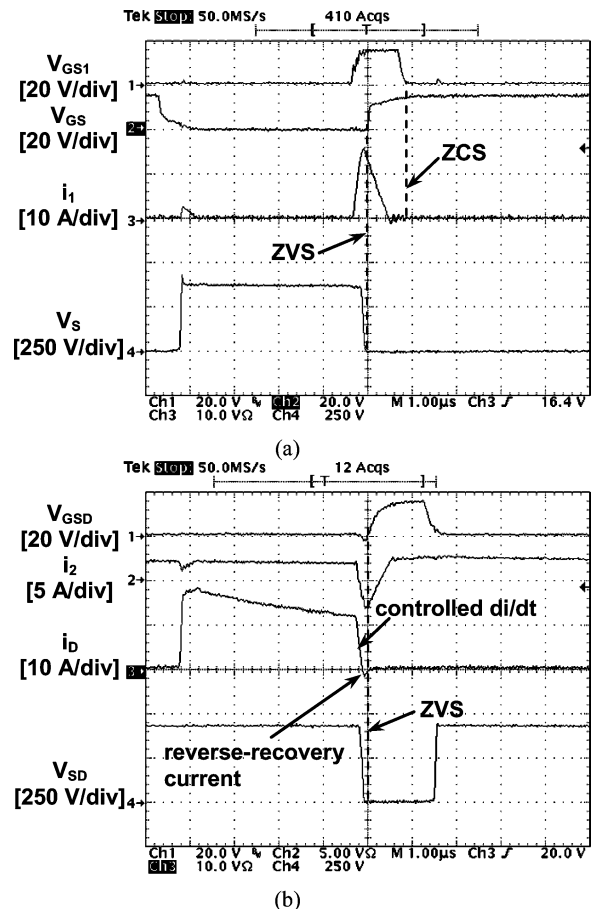


Fig. 10. Measured waveforms of the proposed circuit at $V_{IN} = 90\text{ V}$, $V_B = 380\text{ V}$, $V_O = 430\text{ V}$, $V_{dc} = 12\text{ V}$, $P_{dc} = 700\text{ W}$. Time base: $1\ \mu\text{s}/\text{div}$.

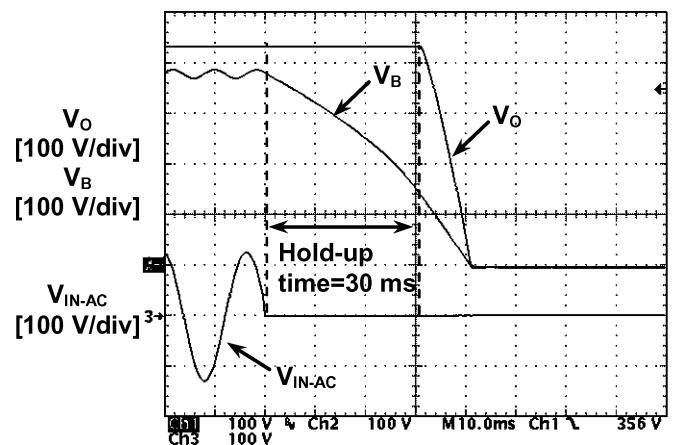


Fig. 11. Measured waveforms of the proposed circuit at full load. Time base: $10\text{ ms}/\text{div}$.

Finally, it should be noted that because of an additional power-processing stage, the efficiency of a three-stage approach may exceed that of a two-stage approach only in applications that are conducive to the three-stage architecture, such as those with an extended holdup time requirement and/or a limited volume for energy-storage (bulk) capacitor. Therefore, a decision to employ a three-stage architecture requires careful consideration

and thorough performance evaluation that takes into account the application/specification requirements as well as design and/or component limitations. Furthermore, since potential efficiency gains of a three-stage approach come at the expense of an increased number of components, a three-stage architecture exhibits a higher cost and may also have slightly reduced power density compared to the conventional two-stage architecture. However, with society's strong push for and commitment to energy savings through the use of more efficient products that is primarily prompted by environmental concerns as well as economic reasons, a slightly increased cost and lower power density of the three-stage architecture may not be any hindrance to its acceptance.

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