Three-Level TAIPEI Rectifier—Analysis of Operation, Design Considerations, and Performance Evaluation

Yungtaek Jang, Fellow, IEEE, Milan M. Jovanović, Fellow, IEEE, Misha Kumar, and Juan M. Ruiz

Abstract—A new low-cost three-phase four-switch three-level zero-voltage-switching (ZVS) discontinuous-current-mode power-factor-correction boost rectifier, for short named the three-level TAIPEI rectifier, that achieves a low input-current total harmonic distortion (THD) and features ZVS of all the switches without any additional soft-switching circuitry was introduced [24]. When designed for Japanese/U.S. nominal three-phase line-to-line voltage 200/240 \( V_{\text{RMS}} \) where 650-V MOSFETs can be used for the two switches, this minimum-component rectifier exhibits excellent performance with the input-current THD below 5% and efficiency in the 96%–97% range, as reported in [25]. However, because the output voltage of the TAIPEI rectifier designed to work with European/U.S nominal line-to-line voltage 380/480 \( V_{\text{RMS}} \) must be at least around 800 V and because the voltage stress of the switches is equal to the output voltage, the rectifier must be implemented with switches that are rated at least 1000 V. As documented in [24], by employing commercially available silicon carbide (SiC) MOSFET switches [26], the rectifier exhibits excellent performance with a full-load efficiency of approximately 98%. However, a relatively high price of SiC switches diminishes the cost effectiveness of the circuit making it less attractive in 380/480-V applications.

In this paper, a low-cost, three-level, ZVS, DCM, PFC boost rectifier that can utilize switches with a lower voltage rating is proposed. In this three-level TAIPEI rectifier, which employs only four switches, the voltage stress across all the switches is clamped to one half of the output voltage. Therefore, the rectifier must be implemented with switches that are rated at least 1000 V. As documented in [24], by employing commercially available silicon carbide (SiC) MOSFET switches [26], the rectifier exhibits excellent performance with a full-load efficiency of approximately 98%. However, a relatively high price of SiC switches diminishes the cost effectiveness of the circuit making it less attractive in 380/480-V applications.

II. THREE-PHASE THREE-LEVEL TAIPEI RECTIFIER

Fig. 1 shows the proposed three-phase three-level ZVS PFC DCM boost rectifier. The input of the circuit consists of three boost inductors \( L_1, L_2, \) and \( L_3 \) coupled to three capacitors \( C_1, C_2, \) and \( C_3 \) connected in the Y (“star”) configuration and the three-phase input terminals through an EMI filter (not shown in Fig. 1). The common point of the capacitors \( N \) is connected to the midpoint between serially connected switch pairs \( S_1 \) and \( S_2 \) and \( S_3 \) and \( S_4 \) and also to the midpoint of split output capacitors \( C_{O1} \) and \( C_{O2} \). The midpoint of serially connected switches \( S_1 \) and \( S_2 \) is connected to output capacitor \( C_{O1} \) through clamping diode \( D_{C1} \) so that the voltage across switch \( S_2 \) is clamped to the voltage across capacitor \( C_{O1} \), which is one-half of output voltage \( V_o \). Similarly, the midpoint of serially connected switches

**Manuscript received November 2, 2015; revised February 2, 2016; accepted March 7, 2016. Date of publication March 17, 2016; date of current version November 11, 2016. This was presented at the Applied Power Electronics Conference, Fort Worth, TX, USA, March 16–20, 2014. Recommended for publication by Associate Editor G. Moschopoulos. The authors are with the Power Electronics Laboratory, Delta Products Corporation, Research Triangle Park, NC 27709 USA (e-mail: yungtaek.jang@deltaww.com; milan.jovanovic@deltaww.com; misha.kumar@deltaww.com; Juan.ruiz@deltaww.com). Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org. Digital Object Identifier 10.1109/TPEL.2016.2543227**
Fig. 1. Proposed three-phase three-level ZVS PFC DCM boost rectifier.

S₃ and S₄ is connected to output capacitor Cₒ₂ through clamping diode Dₒ₂ and the voltage across switch S₃ is also clamped to one-half of output voltage Vₒ. Clamping capacitor Cₘ that is connected between the midpoints of the two pairs of serially connected switches is precharged to its steady-state average voltage of one-half of the output voltage through the loop consisting of capacitor Cₒ₂, the body diode of switch S₂, precharge resistor Rₚₑ, and a winding of coupled inductor Lₘ. Capacitor Cₘ that is used to reset the boost-inductor currents is connected across the serially connected pairs of switches and is decoupled from the output by coupled inductor Lₘ. Its average voltage is equal to the output voltage since the average voltage across the windings of Lₘ is zero. The voltages across switches S₁ and S₄ are clamped to the difference of the voltages across capacitor Cₘ and Cₘ through the body diodes of switch S₄ and switch S₁, respectively. Since this difference is equal to one-half of the output voltage, the voltages across all four switches in the circuit in Fig. 1 are clamped to one-half of the output voltage. Generally, any kind of switch that is capable of conducting current in both directions and blocking voltage in one direction such as for example a MOSFET or an IGBT with an antiparallel diode is suitable for this application.

To achieve a low input-current THD, high power factor (PF), and a wide-load range soft switching of the switches, the circuit in Fig. 1 must operate in DCM with a low-bandwidth output-voltage control. This control can be implemented by employing various modulation strategies of switches S₁–S₄. Fig. 2(a) shows timing waveforms of the four switches of the circuit in Fig. 1 for conventional switching-frequency modulation. In the switching-frequency modulation in Fig. 2(a), two pairs of switches S₁ and S₂ and S₃ and S₄ are switched in a complementary fashion with a small dead time tₒ between their commutation instants to enable the pair of switches that is about to turn on to achieve ZVS. Since dead time tₒ is very small in comparison with switching period Tₛ, the effect of the dead time is negligible, i.e., it can be assumed that the duty cycle of each switch is approximately 50%. Because the switches of each pair operate with the identical gate signals as shown in Fig. 2(a), this modulation scheme is identical to that of the two-level two-switch ZVS DCM PFC TAIPEI rectifier [24].

Fig. 2(b) shows another modulation method of the switches in the circuit in Fig. 1. In this modulation approach, outer switches S₁ and S₄ are switched at a constant frequency in a complementary fashion with a small dead time, i.e., with approximately 50% duty ratio. The duty ratio of inner switches S₂ and S₃, whose turn-on instants are synchronized with the turn on instants of S₁ and S₄, respectively, is PWM to provide regulation of the output. While the rectifier output voltage can be fully regulated by this constant-frequency PWM control, the rectifier exhibits increased input-current THD and loses ZVS of switches S₁ and S₄ when the duty cycle becomes small. However, by properly combining switching-frequency modulation and PWM, a low THD and wide ZVS range can be achieved with a reduced frequency range, which brings about efficiency improvements at light loads. Namely, since in the output-voltage-regulated converter in Fig. 1, the switching frequency increases as the load decreases, the frequency range can be reduced by employing switching-frequency modulation over the load range from full load down to a predetermined level at light load and resorting to the constant-frequency PWM for the loads below this level. Moreover, by keeping the turn-on times of switches S₂ and S₃ constant and decreasing the switching frequency proportional to the load, i.e., by implementing frequency foldback PWM control, additional reduction of switching-related losses at light loads can be achieved.
Constant-frequency PWM control of the rectifier in Fig. 1 can also be implemented by employing the phase-shift PWM illustrated in Fig. 2(c). In this modulation method, each pair of switches $S_1$ and $S_4$ and $S_2$ and $S_3$ is switched at a constant frequency in a complementary fashion with a fixed duty ratio of approximately 50%. The PWM is achieved by a phase shift of the switching instants of the outer switch $S_1$ and $S_4$ pair with respect to the corresponding switching instants of the inner switch $S_2$ and $S_3$ pair. In this phase-shift PWM, the output voltage is maximum when phase-shift angle $\phi$ is zero and is zero when phase-shift angle $\varphi$ is 180°, i.e., $T_S/2$. By combining the switching-frequency modulation and phase-shift PWM, a control method for the three-level TAIPEI rectifier that provides a low THD and wide ZVS range with a reduced switching-frequency range can be implemented.

### III. ANALYSIS OF OPERATION

Fig. 3 shows a simplified model of the circuit in Fig. 1 along with reference directions of currents and voltages. To simplify the analysis of operation, it is assumed that ripple voltages of the input and output filter capacitors shown in Fig. 1 are negligible so that the voltage across the input and output filter capacitors can be represented by constant-voltage source $V_{AN}$, $V_{BN}$, $V_{CN}$, $V_{O1}$, and $V_{O2}$. Also, it is assumed that in the on-state, semiconductors exhibit zero resistance, i.e., they are short-circuits. However, the output capacitances of the switches are not neglected in this analysis. Coupled inductor $L_C$ in Fig. 1 is modeled as a two-winding ideal transformer with magnetizing inductance $L_M$ and leakage inductances $L_{L1}$ and $L_{L2}$. It should be noted that the average voltage across flying capacitor $C_R$ is equal to output voltage $V_O = V_{O1} + V_{O2}$ and the average voltage across clamping capacitor $C_C$ is equal to one half of output voltage $V_O$. The circuit diagram of the simplified rectifier is shown in Fig. 3. The reference directions of currents and voltages in Fig. 3 correspond to the 60° segments of a line cycle when $V_{AN} > 0$, $V_{BN} < 0$, and $V_{CN} < 0$.

To further facilitate the explanation of the operation, Fig. 4 shows topological stages of the circuit in Fig. 3 during a switching cycle, whereas Fig. 5 shows the power-stage key waveforms. As can be seen from the gate-drive timing diagrams of switches $S_1$–$S_4$ in Fig. 5, in this explanation a combination of switching-frequency modulation and phase-shift PWM is used. In Fig. 5, switches $S_1$ and $S_4$ and switches $S_2$ and $S_3$ operate in a complimentary fashion with a short dead time between their commutation instants, i.e., with a fixed duty ratio of approximately 50%. This gating strategy enable ZVS of the switches that are about to turn on. The output-voltage regulation is primarily done by frequency control, except at light loads and/or high-input voltages where phase-shift PWM control is used.

As shown in Figs. 4(a) and 5, before switch $S_2$ is turned OFF at $t = T_1$, inductor current $i_{L1}$ flows through switches $S_1$ and $S_2$. The slope of inductor current $i_{L1}$ is equal to $V_{AN}/L_1$ and the peak of the inductor current at $t = T_1$ is approximately

$$I_{L1\left(PK\right)} = \frac{V_{AN}}{L_1} \times DT_S$$

where $V_{AN}$ is the line-to-neutral voltage and $T_S$ is the switching period. Because the dead time between turn-off of switch $S_1$ and turn-on of switch $S_4$ is very small in comparison with switching period $T_S$, the effect of the dead time is neglected in (1). During the time period between $T_0$ and $T_1$, current $i_{O1}$ decreases at a rate of $-V_{O1}/(L_M + L_{L1})$, while current $i_{O2}$ increases at a rate of $(V_{CR} - V_{O1})/(L_M + L_{L2})$. Magnetizing current $i_M$ is the difference between currents $i_{O1}$ and $i_{O2}$. It should be noted that the magnetizing inductance value of coupled inductor $L_M$ is designed to be sufficiently large so that the ripple current of the coupled inductor does not significantly affect rectifier operation. As shown in Fig. 1, the two windings of inductor $L_C$ are coupled in such a way as to cancel the magnetic fluxes from the differential current of the two windings so that the large magnetizing inductance can be obtained by a small gap in the core without saturation. Since the effect of the current ripple of currents $i_{O1}$ and $i_{O2}$ is negligible, they are not further discussed, although they are shown in the topological stages in Fig. 4.

At $t = T_1$, when switch $S_2$ is turned OFF, inductor current $i_{L1}$ starts charging the output capacitance of switch $S_2$, as shown in Fig. 4(b). Because the sum of the voltages across switch $S_2$ and switch $S_1$ is clamped to clamping capacitor voltage $V_{CC}$, the output capacitance of switch $S_2$ discharges at the same rate as the charging rate of the output capacitance of switch $S_2$. This period ends when the output capacitance of switch $S_2$ is fully charged and clamping diode $D_{C1}$ starts to conduct at $t = T_2$, as shown in Figs. 4(c) and 5. After $t = T_2$, switch $S_3$ is turned ON with ZVS.

Because clamping diode $D_{C1}$ is forward biased, inductor current $i_{L1}$ begins to linearly decrease. The slope of inductor current $i_{L1}$ is equal to $(V_{AN} - V_{O1})/L_1$ and the inductor current at $t = T_3$ is approximately

$$i_{L1\left(t=T_3\right)} = \frac{V_{AN} - (1 - 2D)V_{O1}}{2L_1} \times T_S.$$  

At $t = T_3$, when switch $S_1$ is turned OFF, inductor current $i_{L1}$ starts charging the output capacitance of switch $S_1$, as shown in
Fig. 4. Topological stages of the proposed rectifier when $V_{AN} > 0$, $V_{BN} < 0$, and $V_{CN} < 0$. (a) $[T_0 - T_1]$. (b) $[T_1 - T_2]$. (c) $[T_2 - T_3]$. (d) $[T_3 - T_4]$. (e) $[T_4 - T_5]$. (f) $[T_5 - T_6]$. (g) $[T_6 - T_7]$. (h) $[T_7 - T_8]$. (i) $[T_8 - T_9]$. (j) $[T_9 - T_{10}]$. (k) $[T_{10} - T_{11}]$. (l) $[T_{11} - T_{12}]$. (m) $[T_{12} - T_{13}]$. (n) $[T_{13} - T_{14}]$. (o) $[T_{14} - T_{15}]$.

Fig. 4(d). Because the sum of the voltages across switch $S_1$ and switch $S_4$ is clamped to the voltage difference between flying capacitor voltage $V_{CR}$ and clamping capacitor voltage $V_{CC}$, the output capacitance of switch $S_4$ discharges at the same rate as the charging rate of the output capacitance of switch $S_1$. This period ends when the output capacitance of switch $S_4$ is fully discharged and the antiparallel body diode of switch $S_4$ starts to conduct at $t = T_4$, as shown in Figs. 4(e) and 5. At $t = T_5$, switch $S_4$ is turned ON with ZVS and inductor current $i_{L1}$ is commutated from the antiparallel body diode of switch $S_1$ to the switch, as illustrated in Fig. 4(f). Because the body diode of switch $S_4$ is forward biased and switch $S_2$ is ON, inductor currents $i_{L2}$ and $i_{L3}$ begin to linearly increase after $t = T_4$. At $t = T_5$, switch $S_4$ is turned ON with ZVS and inductor currents $i_{L2}$ and $i_{L3}$ are commutated from the antiparallel body diode of switch $S_4$ to the switch, as illustrated in Fig. 4(f). This period ends when inductor current $i_{L1}$ decreases to zero at $t = T_6$. To maintain DCM operation, minimum voltage $V_{CR(MIN)}$ across flying capacitor $C_R$, which is equal to output voltage $V_O$, is

$$V_{CR(MIN)} = \frac{V_{AN(PK)}}{1 - D} = \frac{\sqrt{2}}{\sqrt{3}(1 - D)} \times V_{L-RMS}$$

(3)
where $V_{AN(PK)}$ is the peak line-to-neutral voltage. It should also be noted that because during the $T_6-T_7$ interval inductor currents $i_{L2}$ and $i_{L3}$ flow in the opposite direction from inductor current $i_{L1}$, the average current through switches $S_3$ and $S_4$ is reduced so that the switches in the proposed rectifier exhibit reduced power losses.

During the time period between $t = T_6$ and $t = T_7$, inductor currents $i_{L2}$ and $i_{L3}$ continue to flow through switches $S_3$ and $S_4$, as illustrated in Fig. 4(b). As shown in Fig. 5, the slopes of inductor currents $i_{L2}$ and $i_{L3}$ are equal to $-V_{BN}/L_2$ and $-V_{CN}/L_3$, respectively. The peaks of the inductor currents at the moment when switch $S_4$ turns off at $t = T_7$ are approximately

$$I_{L2(PK)} = \frac{V_{BN}}{L_2} \times DT_S$$

and

$$I_{L3(PK)} = \frac{V_{CN}}{L_3} \times DT_S.$$  (4)

As it can be seen in (1), (4), and (5), the peak of each inductor current is proportional to its corresponding input voltage as long as duty cycle $D$ and switching period $T_S$ are constant during one-half of the line cycle.

After switch $S_3$ is turned OFF at $t = T_7$, inductor currents $i_{L2}$ and $i_{L3}$ start to simultaneously charge the output capacitance of switch $S_3$ and discharge the output capacitance of switch $S_2$, as shown in Fig. 4(h). This period ends at $t = T_8$ when the output capacitance of switch $S_3$ is fully charged and clamping diode $D_{C2}$ starts to conduct at $t = T_8$, as shown in Figs. 4(i) and 5. After $t = T_8$, switch $S_2$ is turned ON with ZVS.

Because clamping diode $D_{C2}$ is forward biased, inductor currents $i_{L2}$ and $i_{L3}$ begin to linearly increase. This period ends when inductor current $i_{L3}$ reaches zero at $t = T_9$. The slopes of inductor currents $i_{L2}$ and $i_{L3}$ are equal to $(-V_{BN} + V_{O2})/L_2$ and $(-V_{CN} + V_{O2})/L_3$, respectively. Inductor current $i_{L2}$ at $t = T_{10}$ when switch $S_4$ turns off is approximately

$$i_{L2}|_{t=T_{10}} = -\frac{V_{BN} + (1 - 2D)V_{O2}}{2L_2} \times T_S.$$  (5)

At $t = T_{10}$, when switch $S_4$ is turned OFF, inductor current $i_{L2}$ starts charging the output capacitance of switch $S_3$, as shown in Fig. 4(k). Because the sum of the voltages across switch $S_1$ and switch $S_4$ is clamped to the voltage difference between flying capacitor voltage $V_{CR}$ and clamping capacitor voltage $V_{CC}$, the output capacitance of switch $S_1$ discharges at the same rate as the charging rate of the output capacitance of switch $S_3$. This period ends when the output capacitance of switch $S_1$ is fully discharged and the antiparallel body diode of switch $S_1$ starts to conduct at $t = T_{11}$, as shown in Figs. 4(l) and 5. At $t = T_{11}$, switch $S_1$ is turned ON with ZVS and inductor currents $i_{L2}$ is commutated from the antiparallel body diode of switch $S_1$ to the switch, as illustrated in Fig. 4(m). Because switches $S_1$ and $S_2$ are ON, inductor current $i_{L1}$ begins to linearly increase after $t = T_{11}$. During period $T_{12}-T_{13}$, increasing inductor current $i_{L2}$ continues to flow through switches $S_1$ and $S_2$, as shown in Fig. 4(m). Finally, after inductor current $i_{L2}$ reaches zero at $t = T_{13}$, a new switching cycle begins, as shown in Fig. 4(n).

Since in the circuit shown in Fig. 1, the charging current of each boost inductor during the time when the related switch is on is proportional to its corresponding phase voltage and its discharging current proportional to the difference of flying capacitor voltage $V_{CR}$ and the corresponding phase voltage, as shown in the inductor-current waveforms in Fig. 5, average inductor current $<I_{L_{AVG}}>_{T_s}$ of each boost inductor during a switching cycle is

$$<I_{L_{AVG}}>_{T_s} = \frac{2\sqrt{2}V_{L_{N,RMS}}I_{RMS} \sin \omega t}{\sqrt{2V_{L_{N,RMS}}I_{RMS}} \sin \omega t}$$

where $L = L_1 = L_2 = L_3$, and $\omega$ is the angular frequency of the line voltage. For maximum duty cycle $D_{MAX} = 0.5$, average inductor current $<I_{L_{AVG}}>_{T_s,D=0.5}$ of each boost inductor...
during a switching cycle is
\[
\langle I_{L(AVG)} \rangle_{T_s,D=0.5} = \frac{T_s}{8L} \left( \frac{V_{CR} \times \sqrt{2} V_{L,N,RMS} \sin \omega t}{V_{CR} - \sqrt{2} V_{L,N,RMS} \sin \omega t} \right).
\]

By defining input-to-output voltage conversion ratio \( M \) as
\[
M = \frac{V_D}{\sqrt{2} V_{L,N,RMS}}
\]and recalling that the voltage across flying capacitor \( C_R \) is equal to output voltage \( V_O \), i.e., \( V_{CR} = V_O \), average inductor current \( <I_{L(AVG)}>_{T_s} \) in (7) can be rewritten as
\[
\langle I_{L(AVG)} \rangle_{T_s} = \frac{V_O T_s}{32L} \left( \frac{2(1 + 4D^2) \sin \omega t - (1 - 2D)^2 M}{M - \sin \omega t} \right)
\]
i.e., for \( D_{MAX} = 0.5 \)
\[
\langle I_{L(AVG)} \rangle_{T_s,D=0.5} = \frac{V_O T_s}{8L} \left( \frac{\sin \omega t}{M - \sin \omega t} \right).
\]

The current distortion of the average inductor current in (11) is brought about by the denominator term \((M - \sin \omega t)\) and it is dependent on voltage-conversion ratio \( M \). It should be noted that the current distortion of the average inductor current is also dependent on duty cycle \( D \) if duty cycle \( D \) is less than 0.5 as shown in (10).

Fig. 6 shows calculated average boost inductor current \( <I_{L(AVG)}>_{T_s} \) with duty cycle \( D = 0.5, D = 0.2 \), and \( D = 0.1 \) for various input-to-output voltage conversion ratios \( M \). The harmonic content of the average inductor currents shown in Fig. 6 is summarized in Table I. As can be seen from Table I, the third harmonic is the dominant distortion component. However, since in the three-wire power systems, the neutral wire is not available (or not connected), the line currents cannot contain the triplen harmonics (the third harmonic and the odd multiples of the third harmonic). As a result, the proposed circuit exhibits a very low THD and high PF since according to Table I, the remaining harmonics contribute less than 3% of total current distortion up to \( D = 0.2 \). It should be noted that since the line currents cannot contain the third harmonic, the third harmonic of the inductor currents flow through filter capacitors \( C_1 - C_3 \).

Finally, it should be noted that the proposed rectifier automatically balances the voltages across the two output capacitors, i.e., no additional voltage-balancing circuit is required. Natural voltage balancing is achieved because in the circuit in Fig. 1, the average voltages \( V_{O1} \) and \( V_{O2} \) across capacitors \( C_{O1} \) and \( C_{O2} \) are equal to the average voltages across corresponding serially connected switch pairs \( S_1 \) and \( S_2 \) and \( S_3 \) and \( S_4 \) since the average voltages across the windings of inductor \( L_C \) are zero. Because switch pairs \( S_1 \) and \( S_2 \) and \( S_3 \) and \( S_4 \) are operated symmetrically, their average voltages are equal to \( V_{CR}/2 \) so that \( V_{O1} = V_{O2} = V_{CR}/2 \). It should be also noted that clamping voltage \( V_{CC} \) is equalized to \( V_{O2} \) through clamping diode \( D_{C2} \) whenever switch \( S_2 \) is turned ON. Clamping voltage \( V_{CC} \) is also equalized to \( V_{O1} \) through clamping diode \( D_{C1} \) when switch \( S_3 \) is turned ON. As a result, the voltages across capacitors \( C_C \), \( C_{O1} \), and \( C_{O2} \) are equal to one-half of output voltage \( V_O \).

### IV. Design Considerations

In this section, design guidelines for the proposed rectifier are outlined using the example prototype circuit that is evaluated in Section V. The evaluation prototype of the 6-kW three-phase three-level TAIPEI rectifier has been designed and built according to the following key specifications:
Input voltage $V_{IN}$: three-phase, three-wire, 340–520 $V_{L-L, \text{RMS}}$.

Output voltage $V_O$: 780 $V_{DC}$.

Output power $P_O$: 6 kW at nominal input $(380–480 V_{L-L, \text{RMS}})$, 5.4 kW at $V_{IN} = 340V_{L-L, \text{RMS}}$.

Efficiency $\eta$: >97% above 50% load.

Input-current THD: <5%.

PF: <98%.


### A. Switching-Frequency Selection

Because the proposed rectifier employs variable switching-frequency control, both its minimum and maximum switching frequency, i.e., its frequency range, need to be selected. Generally, the selection of the minimum switching frequency is based on the tradeoff between efficiency and size, i.e., power density, whereas the maximum frequency is primarily determined considering limitations imposed by high-frequency switching losses and/or gate-drive capability.

In this design, the minimum frequency, which occurs at the minimum input voltage and full load is set at 20 kHz, which is about the lowest frequency that can make the prototype meet the specified power density. The maximum frequency is set to 250 kHz to primarily limit the switching frequency related losses. With the 250-kHz limit, the prototype rectifier can regulate the output voltage at high line down to 10% load. For loads below 10% of the full load, the burst mode or PWM operation can be applied.

### B. Boost Inductor Design

Based on derivations in [24], the approximate value of boost inductance $L = L_1 = L_2 = L_3$ is given by

$$L \approx \frac{3 \cdot V_{O}^2}{8 \cdot f_S \cdot M \cdot P_O} \times \frac{0.48}{M \cdot 0.92}$$

(12)

where $P_O$ is the output power and $M$ is defined in (9).

For selected switching frequency of 20 kHz at full load of 6 kW and the minimum nominal input voltage $380 V_{L-L, \text{RMS}}$, the required value of the boost inductors is approximately $L = 170 \mu H$. When selecting the core material for the boost inductors, it should be taken into consideration that the rectifier operates in DCM so that the pulsating currents of the boost inductors produce significantly higher core losses compared to those in continuous-conduction-mode operation. In addition, to achieve a low THD, it is necessary to maintain constant slopes of the boost-inductor currents, i.e., it is desirable that inductance value does not change with the inductor current. As a result, ferrite cores with an air gap are the best choice since they offer the lowest core loss and their permeability does not significantly change under the varying magnetic field strength.

To provide packaging flexibility, the boost inductor in each phase of the prototype circuit is implemented by two inductors connected in series. Each inductor was built using a pair of ferrite cores (PQ-40/40, 3C96) with 45 turns of Litz wire (Φ 0.1 mm, 180 strands) and 8.5-mm gaps at inner and outer legs to achieve inductance of 85 $\mu H$. The Litz wire was used to reduce the fringing-effect-induced winding loss near the gap of the inductor cores. For this inductor design, the maximum flux density which occurs at full load and the minimum input voltage is approximately 0.32 T.

### C. Coupled-Inductor Design

The magnetizing inductance of coupled inductor $L_C$ should be sufficiently large so that the ripple current in the coupled inductor does not significantly affect the rectifier operation. As shown in Fig. 1 by the “dot” convention, the two windings of inductor $L_C$ are coupled so that the magnetic fluxes from the differential current of the two windings are cancelled. As a result, a large magnetizing inductance can be obtained by a small gap in the core without saturation.

Coupled inductor $L_C$ was built using a pair of ferrite cores (ETD-54/28/19, 3C96) with 62 turns of Litz wire (Φ 0.1 mm, 150 strands) for each winding and 0.2-mm gap. The measured magnetizing and leakage inductances are approximately 3 mH and 182 $\mu H$, respectively. Peak magnetizing current $I_{M(PK)}$ that occurs when the switching frequency is minimum is given by

$$I_{M(PK)} = \frac{V_O}{8 \cdot L_M \cdot f_S(\text{MIN})}$$

(13)

where $L_M$ is the magnetizing inductance of coupled inductor $L_C$ and $f_S(\text{MIN})$ is the minimum switching frequency at full load and the minimum input voltage. According to (13), the maximum peak-to-peak magnetizing current at full load (6 kW) and the minimum input voltage ($380V_{L-L, \text{RMS}}$) is approximately 1.63 A. The maximum flux density at steady-state operation is approximately 0.28 T, which gives plenty of margin from the saturation flux of the ferrite core.

### D. Input Capacitor Selection

Input capacitors $C_1$–$C_3$ provide filtering of the switching-frequency ripple of the boost inductor currents and a path for their low-frequency triplen harmonics. Since the magnitude of the triplen harmonic component is much smaller than that of the ac component of the boost-inductor currents, the rating of the input capacitors is essentially determined by the RMS value of the ac component of the peak boost inductor current that occurs at full load and low line. Since in this design, the maximum RMS current of capacitors $C_1$–$C_3$ is approximately 5.5 A, a 5-$\mu F$ low-ESR film capacitor (1300 Vdc/600 Vac, 10.5 A at...
20 kHz, 10 A at 100 kHz, ESR = 9.8 mΩ) was used for each of input filter capacitors $C_1$, $C_2$, and $C_3$.

E. Selection of Other Capacitors

The peak current of flying capacitor $C_R$ is equal to the sum of the ac components of the peak boost inductor current and the peak magnetizing current of coupled inductor $L_C$. Since in this design, the RMS value of the sum does not exceed 11 A, two 5-μF parallel-connected film capacitors (1300 Vdc/600 Vac, 10.5 A at 20 kHz, 10 A at 100 kHz) were used for flying capacitor $C_R$.

The current through clamping capacitor $C_C$ is insignificant because the majority of the clamping current flows through clamping diodes $D_{C1}$ and $D_{C2}$ to the output capacitors. A 1-μF film capacitor (875 Vdc, 5 A at 20 kHz) was used for clamping capacitor $C_C$.

Three 560-μF/450-Vdc capacitors connected in parallel were used for output capacitors $C_{O1}$ and $C_{O2}$. Because of additional filtering by the leakage inductance of coupled inductor $L_C$ and capacitor $C_R$, the RMS current through output capacitors $C_{O1}$ and $C_{O2}$ is small.

F. Semiconductor Device Selection

Because the voltage stress of switches $S_1$–$S_4$ is approximately equal to one-half of output voltage $V_O$, i.e., it is around 390 V, it is necessary to use switches that are rated at least 500 V to maintain desirable design margin of 20%. The switches conduct the peak current of approximately 32 A. As a result, in the prototype circuit a IPW65R041CFD MOSFET ($V_{DS} = 650$ V, $R_{DS} = 0.041$ Ω, $C_{OSS} = 400$ pF, $Q_{rr} = 1.9$ μC) from Infineon was used for each switch.

Since input diodes $D_1$–$D_6$ must block the peak voltage that is approximately equal to output voltage $V_O$, i.e., it is around 780 V, and conduct the peak current (approximately 16 A), an C4D20120D diode ($V_{RRM} = 1200$ V, $I_{F_{AVM}} = 20$ A) from Cree was used for each diode.

G. Control Implementation

The control of the prototype rectifier was implemented by TMS320F28027 DSP from TI. Since the rectifier naturally provides tracking of the average inductor current with the corresponding phase voltage, this DSP control consists only of a low-bandwidth feedback loop that regulates the output voltage.

Fig. 7 shows a simplified block diagram of the controller. As it can be seen in Fig. 7, variable-frequency control is implemented by a voltage-controlled oscillator (VCO) whose frequency is determined by the output $V_{CTRL}$ of voltage controller $G_C$ which processes the error between sensed output voltage $V_{O(SEN)}$ and its reference $V_{O(REF)}$. In addition, the controller implements soft start and frequency-foldback control by employing a combination of frequency modulation and phase-shift PWM. Although soft-start control can be implemented by switching-frequency control alone, i.e., by slowly decreasing...
the switching frequency from the maximum frequency toward the required control frequency, combining it with PWM control enables more controllable and smooth start up. However, the frequency foldback control that is used to extend the minimum-load regulation range and/or improve light-load efficiency requires PWM control. Namely, frequency-foldback mode, i.e., the operation where the switching frequency is decreased as the load is reduced, can only be implemented if PWM control is also employed to provide regulation at a reduced output power.

In the implementation also shown in Fig. 7, the drive signals of switches $S_1$–$S_4$ are obtained by using digital pulse-width modulator (DPWM) with two identical synchronized digital carrier ramps that are generated by counting DSP clock periods $T_{CLK}$. Since the carrier ramp period $T_S = N_{CAR}T_{CLK}$, where $N_{CAR}$ is the number of clock periods, carrier frequency $f_S$ is proportional to $1/N_{CAR}$. As shown in Fig. 7, the ramp frequency is set by multiplexer MUXFREQ that based on the state of soft-start flag $Flag_{SS}$ and frequency-foldback flag $Flag_{FB}$ selects either the frequency of VCO, or the frequency of frequency-foldback VCOFB, or the frequency of the soft-start circuit. The number of clock periods $N_{CAR}$ is obtained by finding the reciprocal value of the MUXFREQ output.

The VCO transfer function is set by the selection of its maximum frequency $f_{MAX}$, i.e., minimum count number $N_{MIN}$, and gain $K_{VCO}$. According to Fig. 7, the VCO output is given by

$$
\frac{1}{N_{VCO}} = \frac{1}{N_{MIN}} - K_{VCO} \cdot V_{CTRL}. \quad (14)
$$

Since

$$
\frac{1}{N_{VCO}} = T_{CLK} \cdot f_{VCO} = \frac{f_{VCO}}{f_{CLK}} \quad (15)
$$

and

$$
\frac{1}{N_{MIN}} = T_{CLK} \cdot f_{MAX} = \frac{f_{MAX}}{f_{CLK}} \quad (16)
$$

relationship in (14) can be written as

$$
\frac{f_{VCO}}{f_{CLK}} = \frac{f_{MAX}}{f_{CLK}} - K_{VCO} \cdot V_{CTRL}. \quad (17)
$$

As it can be seen from (17), the normalized frequency of the VCO with respect to $f_{CLK}$ is a linear function of control voltage $V_{CTRL}$ with negative slope $K_{VCO}$. As a result, the VCO frequency increases as the control voltage decrease, i.e., as the load current decreases.

The drive signals of complementary switches $S_1$ and $S_4$ that always operate with 50% duty cycle are obtained by comparing the carrier ramp with one-half of its count value $N_{CAR}$, i.e., with $0.5N_{CAR}$, as shown in Fig. 7. The drive signals of complementary switches $S_2$ and $S_3$ that also always operate with 50% duty cycle but also can be phase shifted with respect to switches $S_1$ and $S_4$ are obtained by comparing the carrier ramp with $0.5N_{CAR} - N_{PS}$ and $N_{CAR} - N_{PS}$, where $N_{PS}$ is proportional to phase shift $\varphi$, i.e., $N_{PS} = (\varphi/360)N_{CAR}$. Since the $N_{PS}$ range is from 0 to $0.5N_{CAR}$, phase shift $\varphi$ is in the $0^\circ$–$180^\circ$ range. The $N_{PS}$ value that is selected by MUXPS is determined either by the soft start or frequency foldback circuit.

The reason for the ramp comparison with two levels is to preserve 50% duty cycle of switches $S_2$ and $S_3$ during phase-shift operation. Namely, the ramp comparison with $0.5N_{CAR} - N_{PS}$ defines the beginning of the off time, whereas the comparison with $N_{CAR} - N_{PS}$ defines its end. Since the difference between the two levels is $0.5N_{CAR}$, i.e., it is equal to one-half of the digital ramp height, the drive signals for switches $S_2$ and $S_3$ operate with 50% off time, i.e., with 50% duty cycle.

The frequency foldback circuit is activated at light loads whenever output of the controller $V_{CTRL}$ falls below reference level $V_{CTRL(REF)}$ and frequency foldback flag $Flag_{FB}$ is set to 1. The frequency foldback circuit consists of the frequency-foldback VCO, VCOFB, and the preprogrammed phase shift as a function of the VCO’s frequency. The VCOFB transfer function is set by the selection of its minimum frequency, i.e., maximum count number $N_{MAX}$ and gain $K_{VCO}$. It should be noted that opposite from VCO, VCOFB is set up to decrease the frequency as the load decreases, i.e., its normalized frequency is a linear function of control voltage $V_{CTRL}$ with positive slope $K_{VCO}$ given by

$$
\frac{f^{FB}_{VCO}}{f_{CLK}} = \frac{f_{MIN}}{f_{CLK}} + K^{FB}_{VCO} \cdot V_{CTRL}. \quad (18)
$$

In the frequency-foldback mode, the output voltage is regulated by the phase-shift modulation illustrated in Fig. 2(c) by employing open-loop control where the phase shift is preprogrammed as a function of the foldback frequency. Generally, any relationship where the phase shift is monotonically increasing as the foldback frequency decreases can be used.

Fig. 7 shows preprogrammed phase shift dependence on the foldback frequency. As can be seen, the phase shift increases as the foldback frequency decreases. The phase-shift dependence on frequency shown in Fig. 7 is obtained by assuming a linear relationship between phase-shift count $N^{FB}_{VCO}$ and switching-period count $N^{FB}_{SS}$, i.e.,

$$
N^{FB}_{SS} = 0.5(N^{FB}_{VCO} - 240),
$$

where $240 < N^{FB}_{VCO} < 3000$, which corresponds to the 250–20-kHz foldback-frequency range. In the prototype circuit, the maximum phase shift of $\varphi = \frac{N^{FB}_{SS}}{N^{FB}_{VCO}} \cdot 360 = 1440 \text{mm} \cdot 360^\circ = 173^\circ$ was set at minimum frequency $f^{FB}_{VCO} = 20$ kHz. This phase shift corresponds to the minimum duty cycle of $D_{MIN} = 180^\circ - 173^\circ \approx 0.02$.

The start up of the circuit is managed by the soft-start circuit which gradually decreases the switching frequency from the maximum frequency down to that required by the regulation loop. As shown in Fig. 7, soft-start frequency $1/N^{SS}_{SSRamp}$ is decreased by increasing switching period count $N^{SS}_{SSRamp}$ from $N_{MIN}$ to $N_{MAX}$ by one count every time step $t_{step}$. For a given frequency range, i.e., for given $N_{MIN}$ and $N_{MAX}$, the duration of time step $t_{step}$ is determined by desired maximum soft-start duration $T_{SS}$, as $t_{step} = T_{SS}/(N_{MAX} - N_{MIN})$. In the experimental prototype circuit, the frequency soft-start range is from $300(N_{MIN} = 200)$ to 20 kHz ($N_{MAX} = 3000$) and $t_{step} = 2$ ms which results in $T_{SS} = 5.6$ s.

As shown in Fig. 7, during the soft-start normalized soft-start frequency $1/N^{SS}_{SSRamp} = f_{SS}/f_{CLK}$ is compared with VCO’s normalized frequency $1/N_{VCO} = f_{VCO}/f_{CLK}$ and the higher
Fig. 8. Experimental prototype circuit of the proposed rectifier.

Fig. 9. Measured voltage waveforms of clamping capacitor \( C_C \) and output capacitors \( C_{O1} \) and \( C_{O2} \) during start up: (a) after ac source is connected and (b) after controller is turned on. Time scale is 400 ms/div.

Fig. 10. Measured input-current waveforms at full power for three-phase line-to-line RMS input voltage: (a) 380 V and (b) 480 V. Time scale is 5 ms/div.

start up the soft-start frequency is greater than the frequency of VCO, the soft-start circuit determines the switching frequency. When the frequency of VCO becomes larger than the decreasing soft-start frequency, the control loop determines the switching frequency. This implementation of soft start offers seamless transition from the soft start control to the feedback-loop control.

Furthermore to enable as smooth as possible soft-start control, the open-loop phase-shift control is also implemented alongside the frequency-modulation control. As shown in Fig. 7, the preprogrammed soft-start phase shift is maximum at the maximum soft-start frequency and decreases as the soft-start frequency decreases. The phase-shift dependence on frequency shown in Fig. 7 is obtained by assuming a linear relationship between phase-shift count \( N_{PS} \) and switching-period count \( N_{SP} \), i.e.,

\[
N_{PS} = -0.2(N_{SP} - 600), \quad 200 < N_{SP} < 3000,
\]

which corresponds to the 300–20-kHz soft-start frequency range. In the prototype circuit, the maximum phase shift of \( \phi = \frac{N_{PS}}{N_{SP}} \cdot 360^\circ = \frac{200}{2000} \cdot 360^\circ = 144^\circ \) was set at maximum frequency \( f_{SS} = 300 \) kHz. This phase shift corresponds to the minimum duty cycle of \( D_{MIN} = \frac{180^\circ - 144^\circ}{360^\circ} = 0.1 \).

The controller is design by applying analog-redesign approach, i.e., by designing controller \( G_C \) in the \( s \)-domain and
mapping it in the z-domain. The equivalent s-domain voltage-loop gain of the control loop of the experimental converter is

$$T_V(s) = K_D \cdot \frac{1}{FSR} \cdot G_C(s) \cdot K_{VCO} \cdot G_{PS}(s) \cdot e^{-sT_D} \approx K_D \cdot \frac{1}{FSR} \cdot G_C(s) \cdot K_{VCO} \cdot G_{PS}(s)$$  \hspace{1cm} (19)$$

where $K_D$ is the sensing gain of the output voltage, FSR is the full-scale range of analog-to-digital (ADC) converter, $G_{PS}(s)$ is the low-frequency power-stage small-signal transfer function, and $e^{-sT_D}$ is the total digital-loop delay that includes ADC conversion time, DSP computational time, and the delayed update of DPWM to achieve synchronization to the resetting of DPWM ramp. Since in the experimental circuit, the sampling frequency $f_{SAMPL} = 25$ kHz is much greater than the desired 10-Hz bandwidth of the loop, the digital-loop delay can be neglected since it has no measurable effect on the voltage-loop phase margin.

For a resistive load, power stage small-signal transfer function $G_{PS}(s)$ is a single-pole transfer function

$$G_{PS}(s) = K_{PS} \cdot \frac{1}{1 + \frac{s}{2\pi f_{PO}}}.$$  \hspace{1cm} (20)$$

By using small-signal measurements, it was estimated that for the experimental circuit at full power of 6 kW and at line-to-line voltage of 380 V, power-stage gain $K_{PS} = 0.052$ and power-stage pole frequency $f_{PO} = 0.4$ Hz.

To compensate the loop, two-pole one-zero controller, i.e., PI controller with high-frequency pole, was used. The controller’s s-domain transfer function is

$$G_C(s) = \frac{K}{s} \left(1 + \frac{s}{2\pi f_z} \right).$$  \hspace{1cm} (21)$$

To obtain 10-Hz bandwidth, the controller parameters were selected as $K = 36$, $f_z = 2$ Hz, and $f_p = 2$ kHz.

Since the sampling frequency in the prototype circuit is $f_{SAMPL} = 25$ kHz, the controller’s z-domain transfer function obtained by bilinear (Tustin’s) transformation that is coded in the DSP is

$$G_C(z) = 0.201 \cdot \frac{2.882 + 1.448 \cdot 10^{-3} \cdot z^{-1} - 2.881 \cdot z^{-2}}{1 - 1.598 \cdot z^{-1} + 0.598 \cdot z^{-2}}.$$  \hspace{1cm} (22)$$

Finally, it should be noted that the control signals at the output of the DSP controller are coupled to the gate-to-source voltage of the corresponding switches with SI8235 drivers from Silicon Labs and that the output overvoltage protection and switch...
V. EXPERIMENTAL RESULTS

The performance of the proposed rectifier was evaluated on a 6-kW prototype circuit that was designed according to the key specifications listed in Section IV. Fig. 8 shows the power-stage schematics of the experimental prototype circuit along with the component information.

Fig. 9 shows the measured voltage waveforms of clamping capacitor $C_C$ and two serially connected output capacitors $C_{O1}$ and $C_{O2}$ during start up. Because voltages across those capacitors limit the peak voltage stresses of the primary switches, voltages $V_{CC}$, $V_{O1}$, and $V_{O2}$ should always be equal to one half of the output voltage even during the start up. Fig. 9(a) shows the $V_{CC}$, $V_{O1}$, and $V_{O2}$ voltage waveforms immediately after the ac source is connected and Fig. 9(b) shows the same waveforms after the controller is subsequently turned on. As it can be seen from Fig. 9(a) and (b), during the entire start-up period, voltages $V_{O1}$, $V_{O2}$, and $V_{CC}$ are equal to one-half of the output voltage.

Fig. 10(a) and (b) shows the measured input-current waveforms of the experimental circuit operating at full power from 380 $V_{L-L, RMS}$ and 480 $V_{L-L, RMS}$ input, respectively. It should be noted that input currents $i_A$, $i_B$, and $i_C$ are measured between the three-phase ac source and the input EMI filter of the rectifier which is not shown in Fig. 8. The measured full-power THDs of the input currents are below 3% for both input voltages. Fig. 11 shows the measured current waveforms of boost inductors $L_1$, $L_2$, and $L_3$ at full power. The measured waveforms and the ideal waveforms in Fig. 5 differ during the time intervals when the inductor currents are supposed to be zero. This difference is caused by the parasitic resonance of the junction capacitances of the reverse-biased input bridge rectifiers $D_1$–$D_6$ with the boost inductors. This current ringing increases slightly the THD of the input current and, if necessary, can be minimize by selecting rectifiers with smaller junction capacitances. Fig. 12 shows the waveforms of the drain voltages of switches $S_1$–$S_4$. It can be seen that all the switch voltages are well clamped to one half of output voltage $V_O$. 

current overcurrent protection are implemented outside the DSP, i.e., by using analog comparators. Current-sensing transformers with turns ratio 1:100 were used for sensing current of the switches.
The output-voltage regulation in the prototype circuit is implemented by a combination of variable-switching-frequency and phase-shift PWM control. The phase-shift PWM control is employed at light load and can also be employed at high-input voltage to limit the switching-frequency range. Fig. 13(a) shows the waveforms of the drain voltages of switches S1–S4 at full power and 520 \( V_{L-L,RMS} \) input. As it can be seen from Fig. 13(a), in the phase-shift mode, each pair of switches S1 and S4, and S2 and S3, is switched in a complementary fashion with a fixed duty ratio of approximately 50% with the switching instants of the outer switch S1 and S4 pair phase shifted with respect to the corresponding switching instants of the inner switch S2 and S3. Fig. 13(b) shows the measured current waveforms of boost inductors \( L_1, L_2, \) and \( L_3 \) that correspond to voltage waveform seen in Fig. 13(a). The measured waveforms shown in Fig. 13(a) and (b) match well with the ideal waveforms shown in Fig. 5.

The operation of the circuit with unbalanced line voltages is illustrated in Figs. 14 and 15. Fig. 14(a) shows input-current waveforms of the experimental circuit with phase A open. Even under this extreme unbalanced condition, the measured THD of the remaining two phases is below 10%. Fig. 14(b) shows the measured voltage waveforms of clamping capacitor \( C_C \) and two serially connected output capacitors \( C_{O1} \) and \( C_{O2} \) during the same transient of phase A open. As it can be seen from Fig. 14(b), during the entire transient period, voltages \( V_{O1}, V_{O2}, \) and \( V_{CC} \) are well balanced and equal to one-half of the output voltage. Fig. 15(a) and (b) illustrates operation of the circuit with one phase shorted (voltage of phase A set to zero). Under this unbalanced condition, the measured THD of the line currents is still well below 10% and voltages \( V_{O1}, V_{O2}, \) and \( V_{CC} \) are well balanced and equal to one-half of the output voltage as shown in Fig. 15(b).

Tables II and III show measured THD and PF at nominal input voltages, respectively. The proposed rectifier achieves less than 5% input-current THD at the nominal input

<table>
<thead>
<tr>
<th>Output Power [kW]</th>
<th>0.5</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage ( [V_{L-L}] )</td>
<td>380</td>
<td>4.51</td>
<td>4.33</td>
<td>3.91</td>
<td>3.18</td>
<td>3.05</td>
<td>2.78</td>
</tr>
<tr>
<td>480</td>
<td>13.32</td>
<td>9.77</td>
<td>5.48</td>
<td>4.95</td>
<td>4.62</td>
<td>4.39</td>
<td>2.81</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Output Power [kW]</th>
<th>0.5</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage ( [V_{L-L}] )</td>
<td>380</td>
<td>72.07</td>
<td>89.56</td>
<td>96.37</td>
<td>98.33</td>
<td>99.01</td>
<td>99.3</td>
</tr>
<tr>
<td>480</td>
<td>69.97</td>
<td>84.87</td>
<td>93.76</td>
<td>96.95</td>
<td>98.12</td>
<td>98.46</td>
<td>98.89</td>
</tr>
</tbody>
</table>
themselves, and above 50% of the full load. The THD \( V_{\text{THD}} \) was 97.4%, whereas the peak efficiency at \( 380 \) \( V_{L} \) L-RMS is 97.4%. For both input voltages, the peak efficiency occurs at half load.

VI. SUMMARY

In this paper, a new three-phase four-switch three-level ZVS PFC DCM boost rectifier has been introduced and its analysis of operation, design considerations, and performance evaluation have been presented. In the proposed rectifier, all semiconductor switches operate with ZVS and their off-state voltage is always clamped to one-half of the output voltage. To reduce the switching-frequency range and maximize the light-load efficiency, the control is implemented by a combination of variable-switching frequency and phase-shift PWM control.

The proposed soft-switched rectifier exhibits efficiency in the 96%–98% range and achieves less than 5% input-current THD over the nominal input (380–480 \( V_{L} \) L-RMS) and above 50% of the full load. The performance evaluation was done on a three-phase 6-kW prototype designed for the 340–520 \( V_{L} \) L-RMS line-voltage range. The measured full-load input-current THD at 380 \( V_{L} \) L-RMS and 480 \( V_{L} \) L-RMS were 2.5% and 2.9%, respectively. The measured peak efficiency at 480 \( V_{L} \) L-RMS is 98.0%, whereas the peak efficiency at 380 \( V_{L} \) L-RMS is 97.4%.

REFERENCES


JANG ET AL.: THREE-LEVEL TAIPEI RECTIFIER—ANALYSIS OF OPERATION, DESIGN CONSIDERATIONS, AND PERFORMANCE EVALUATION 955

Yungtaek Jang (S’92–M’95–SM’01–F’16) was born in Seoul, South Korea. He received the B.S. degree in electrical engineering from Yonsei University, Seoul, in 1982, and the M.S. and Ph.D. degrees in electrical engineering from the University of Colorado, Boulder, CO, USA, in 1991 and 1995, respectively. Since 1996, he has been a Senior Member of the R&D Staff at the Power Electronics Laboratory, Delta Products Corporation, Research Triangle Park, NC, USA—the U.S. subsidiary of Delta Electronics, Inc., Taiwan. He holds 30 U.S. patents, and has published 31 journal articles in refereed journals and more than 50 technical papers in conference proceedings.

Dr. Jang received the IEEE Transactions on Power Electronics Prize paper awards for the best paper published in 1996, 2009, and 2013, respectively.
Milan M. Jovanović (S’85–M’88–SM’89–F’01) was born in Belgrade, Serbia. He received the Dipl.Ing. degree in electrical engineering from the University of Belgrade, Belgrade, and the Ph.D. degree in electrical engineering from Virginia Tech, Blacksburg, VA, USA. He is currently the Senior Vice President for R&D of Delta Products Corporation, Research Triangle Park, NC, USA—the U.S. subsidiary of Delta Electronics, Inc., Taiwan, one of the world’s largest manufacturers of power supplies. Dr. Jovanović is a Member of the U.S. National Academy of Engineering.

Misha Kumar was born in New Delhi, India, in 1987. She received the B.Tech. degree in power-electrical engineering from Guru Gobind Singh Indraprastha University, Delhi, in 2009, and the M.S.E.E degree from North Carolina State University (NCSU), Raleigh, NC, USA, in 2011. During her graduate studies, she worked as a summer Research Assistant at FREEDM System Center, NCSU. Since August 2011, she has been a Member of the R&D Staff at Delta Power Electronics Laboratory, Delta Products Corp, Research Triangle Park, NC. Her current research interests include analysis, modeling, simulation, and design of digital control of power converters especially single-phase, three-phase boost PFC rectifiers, and gradient power supplies for MRI applications.

Juan M. Ruiz was born in Pereira, Colombia. From 1996–1999, he studied electronics technology from Caldas University, Pereira. From 1995 to 1998, he was a Research Technician for Electronica and Computadores Magazine sponsored by CEKIT.SA. From 2002 to 2003, he was a Senior Engineering Technician at Raltron Electronics, Miami, FL, USA. From January 2008 to June 2008, he was a qualification Technician with IBM. In September 2008, he joined Delta Power Electronics Lab, Research Triangle Park, NC, USA, where he is currently a Support Engineer.